Gate-All-Around Devices and Circuits

(Research contract F 61708-92-C0041)

First Year Report

by:

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J.P. Eggermont, D. Flandre and X. Baie

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The goal of this research activity is to improve the GAA technology, to apply it to the fabrication of CMOS circuits and to assess the radiation hardness of the devices. The test vehicle is a 1k SRAM which has to be demonstrated by September 1994. In the first year of activity, we have worked on the following topics: assessment of the pre-rad and post-rad characteristics of the transisters, improvement of processing (reduction of the gate oxide thickness, circuit design including issues aimed at improving the total-dose hardness.

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Content

1. Introduction

The goal of this research activity is to improve the GAA technology, to apply it to the fabrication of CMOS circuits and to assess the radiation hardness of the devices. The test vehicle is a 1k SRAM which has to be demonstrated by September 1994. In the first year of activity, we have worked on the following topics:

- Assessment of the pre-rad and post-rad characteristics of the transistors
- Improvement of processing (reduction of the gate oxide thickness)
- Circuit design, including issues aimed at improving the total-dose hardness

2. Preliminary device irradiation results

These results are based on GAA devices fabricated at the Micrelectronics Lab of the UCL in early 1992 (before the current program got started).

2.1. Effect of Total-Dose Irradiation on GAA Devices

2.1.1. Introduction

Silicon-on-Insulator (SOI) technology is increasingly used to produce rad-hard integrated circuits. Indeed, devices produced using this technology are inherently hardened against SEU and gamma-dot events [1], and excellent total-dose hardening can be obtained when a suitably hardened process is used. SOI microprocessors withstanding doses of over 100 Mrad(SiO_2) have already been reported [2]. Classical lateral isolation of devices using LOCOS or oxidized mesa [3] is inherently soft, since it comprises a rather thick oxide which is of lesser quality than the gate oxide, and, therefore, gives rise to large threshold voltage shifts at the edge of the devices upon irradiation. In n-channel bulk devices a rather heavy boron field implant dose is used to increase the threshold of the lateral transistor such as to avoid edge transistor turn-on and to achieve inter-device isolation. This edge leakage suppression technique is less effective in SOI devices since most of the implanted boron segregates into the field oxide during the LOCOS formation process. Therefore, specially designed SOI transistors, such as edgeless devices [4], H-gate MOSFETs [5] and n-channel devices with heavy P^+-edge channel-stop doping at the source [2] are used in order to suppress the edge leakage problem. All these types of device, however, consume significantly more silicon real estate than regular MOSFETs, which reduces packing density.
The gate-all-around (GAA) MOSFET is a device where the silicon in the channel area is completely wrapped by the gate oxide and the gate electrode material [6]. Hence, unlike in regular transistors, there is no contact between a field oxide and the active silicon, and the only radiation-generated charges that will influence the device electrical characteristics are found in the high-quality gate oxide.

2.1.2. Device fabrication

The devices were fabricated using a simple 3 µm process and commercial 75 mm SIMOX substrates. The original thickness of the silicon film is 180 nm. This silicon overlayer is first thinned down using oxidation and oxide strip in buffered HF in order to obtain a device silicon film thickness of 80 nm at the end of the process. A thin pad oxide is grown, and silicon nitride is deposited. Using a mask step, the nitride, the pad oxide and the silicon film are patterned to define the active areas. An oxidation step (200 nm oxide) is used to round the edges of the silicon islands, after which the nitride and the pad oxide are stripped. A mask step is then used to cover the entire wafer with resist except areas which correspond to an oversize of the intersection between the active area

and the poly gate layers. The wafers are then immersed in buffered HF. At this step the oxide on the sidewalls of the silicon islands as well as the buried oxide are etched, and a cavity is created underneath the center part of the silicon islands (Figure 1).

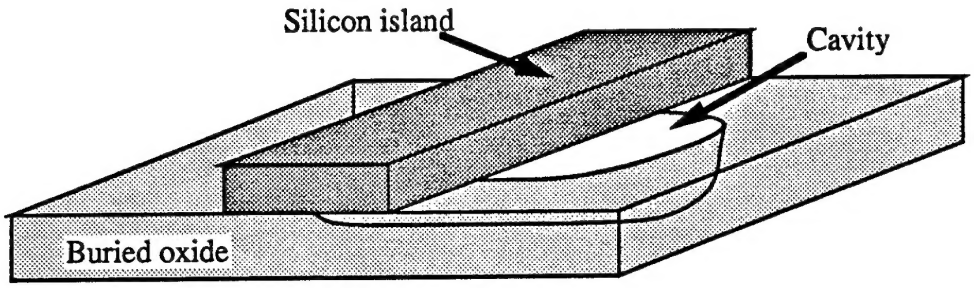

Figure 1: Formation of the Gate-all-Around device: formation of a silicon-on-insulator island and etching of a cavity below it.

Gate oxidation is then carried out. In this step, a 50 nm-thick gate oxide is grown over all the exposed silicon (top, bottom and edges of the active silicon, as well as on the silicon substrate in the bottom of the cavity). Boron is implanted to adjust the threshold voltage, and polysilicon gate material is then deposited and doped n-type. Because of the extremely good conformality of LPCVD polysilicon, the gate oxide over the cavity is completely coated with polysilicon, and a gate is formed on the top, the sides and the bottom of the channel area (hence the name of gate-all-around (GAA) device). The polysilicon gate is then patterned using conventional lithography and anisotropic plasma etch. Source and drain are formed using phosphorous implantation followed by an annealing step. At this time, the GAA transistor structure is formed (Figure 2) . In order to complete the process a CVD oxide layer is deposited, and contact holes are opened. An aluminum metallization step is then used to contact the devices.

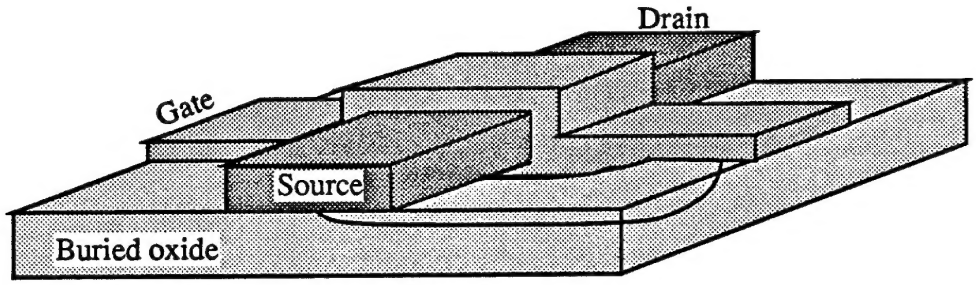

Figure 2: Formation of the Gate-all-Around device: the complete transistor structure.

2.1.3. Device characteristics

The device characteristics of GAA devices above threshold have been presented experimentally and theoretically [6,7]. This type of device exhibits a transconductance and a current drive which can be up to 3 to 4 times higher than that of a regular transistor, due to the presence of two channels and to volume inversion. The n-channel devices presents, however, an unexplained kink in the $I_D(V_G)$ curve around threshold (Figure 3).

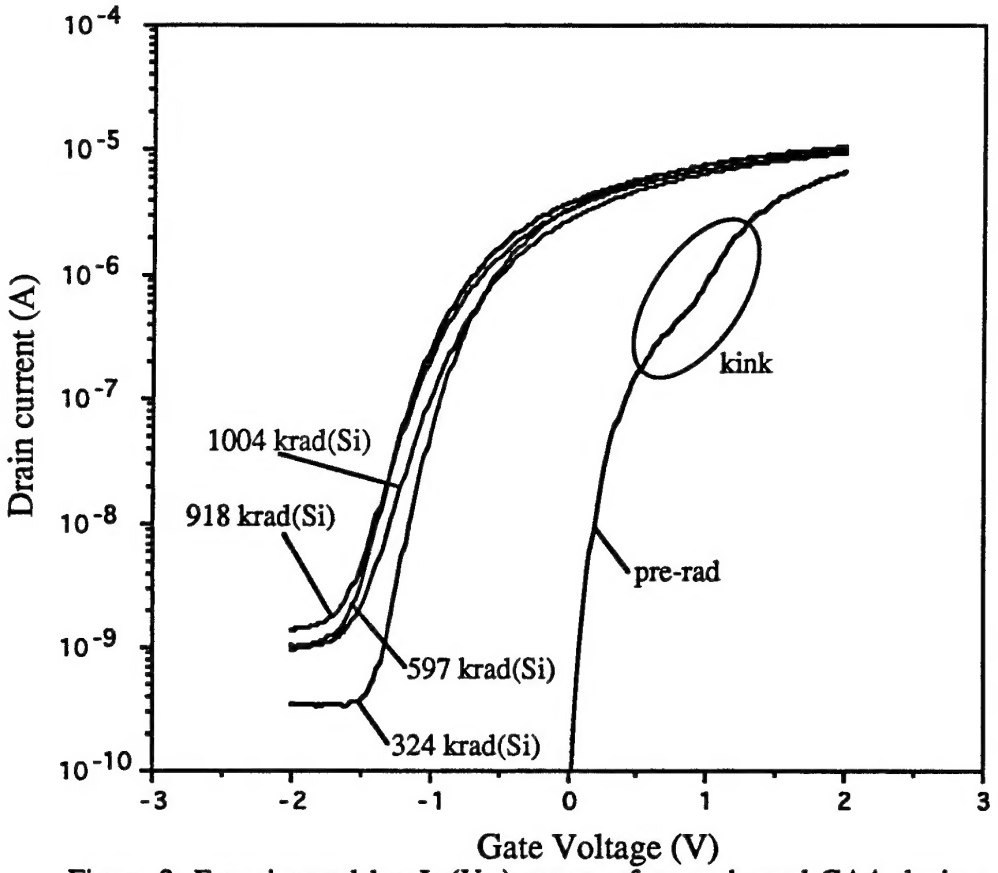

Figure 3: Experimental log $I_D(V_G)$ curves of an n-channel GAA device exposed to different irradiation doses. V_G=3 V during ^{60}Co irradiation, and V_{DS}=0.5 V during parameter extraction. W/L=3μm/3μm.

As we shall see in the device simulation Section, this kink is due to parasitic conduction at the edges of the device. In a linear $I_D(V_G)$ plot, this effect shows as a current increase before threshold (threshold voltage is 1 volt - Figure 4).

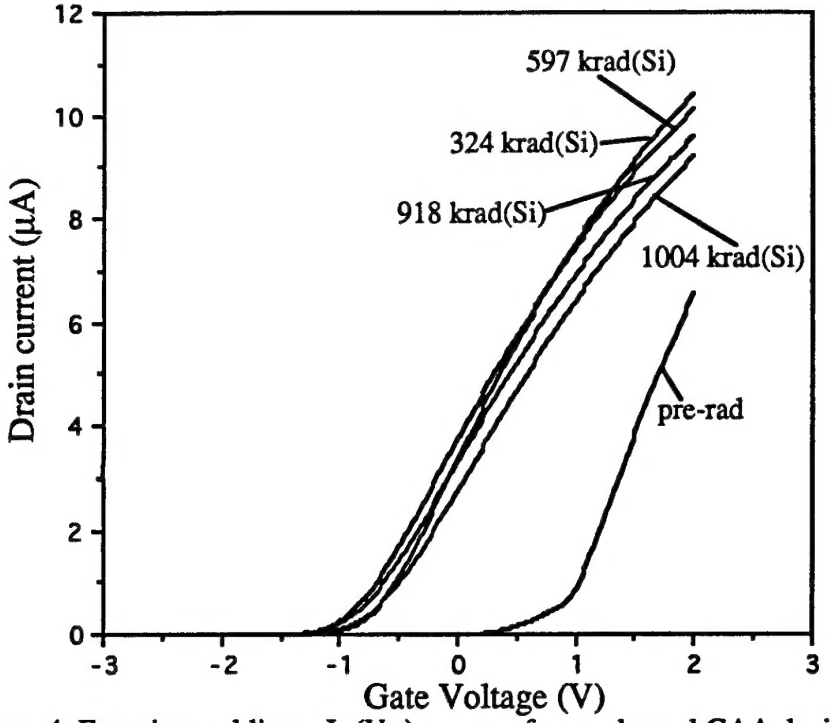

Figure 4: Experimental linear $I_D(V_G)$ curves of an n-channel GAA device exposed to different irradiation doses. V_G=3 V during ^{60}Co irradiation, and V_{DS}=0.5 V during parameter extraction. W/L=3μm/3μm.

This phenomenon is explained by the lower threshold voltage at the edges of the device than in the top and bottom interfaces. Strangely enough, the edge leakage seems to disappear when the device is irradiated. Figures 3 and 4 present the $I_D(V_G)$ characteristics of a 3μm x 3μm device before irradiation and after irradiation to doses of 324, 597, 918 and 1004 krad(Si) using a ^{60}Co source. The devices were measured *in situ* using an HP4145 semiconductor parameter analyzer and 5-meter long coaxial cables passing through the irradiation chamber walls. All measurement could therefore be carried out without interrupting the irradiation process. The gate was held at +3 volts during irradiation, with all other terminals grounded. This configuration (gate high) has been show in the past to be the worst-case irradiation bias condition [10]. The $I_D(V_G)$ curves were measured in the linear regime with V_{DS}=50 mV. It can be seen on Figure 1 that none of the curves measured after irradiation present a kink. This behaviour of the GAA device is opposite to what is observed in regular SOI MOSFETs where the edge transistor threshold voltage shifts more than the main device threshold upon irradiation, thereby increasing the kink in the subthreshold $I_D(V_G)$ characteristic [8] (Figure 4b). The increase of the OFF background current (up to 1 nA) for negative gate biases is not due to a loss of gate control. It is most likely due to the increase of the fast surface-state density at the Si-SiO_2 interface in contact with the drain-body junction upon irradiation. Indeed, such states are known to increase the surface generation velocity, which in turn increases the drain junction leakage.

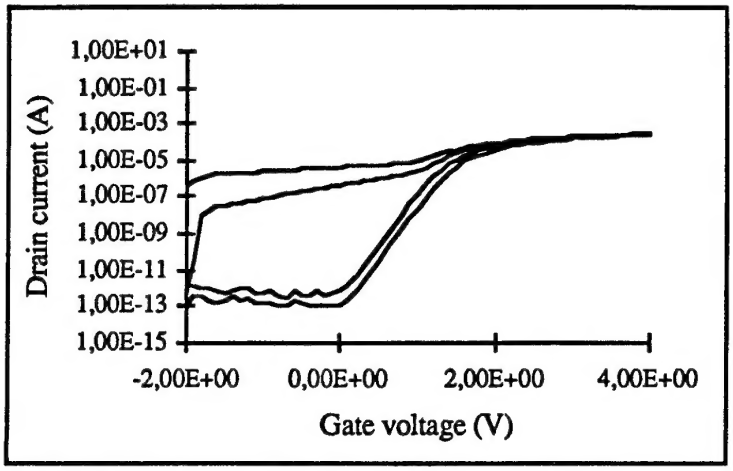

Figure 4b: Standard n-channel device, W/L=20/1, irradiated with the following doses: 0, 10, 50 and 100 krad(Si) (from right to left). The 250Å-gate oxide was grown at 850°C.

2.1.4. Device simulation

The three-dimensional numerical device simulator DAVINCI [9] was used to explain the device behaviour. The simulated GAA device has the same parameters as the measured device, *i.e.*:W=L=3 μm, t_{si}=80 nm, t_{ox}=50 nm, N_a=1.3x10^{17}cm^{-3}. The gate material is N^+ polysilicon. A regular SOI MOSFET was simulated as well. This transistor is an oxidized mesa device without overdoping of the mesa sidewalls. The silicon film thickness is 160 nm, N_a=1.0x10^{16}cm^{-3} up to a depth of 120 nm and N_a=3.0x10^{17}cm^{-3} for depths between 120 nm and 160 nm. This box doping profile gives the device the same threshold voltage (1 V) as the GAA device and prevents back-gate leakage upon irradiation. The buried oxide thickness, the gate oxide thickness, and the sidewall oxide thickness are 400 nm, 50 nm and 200 nm, respectively. The thickness of the lateral oxide is similar to that used in [3]. The meshes used for the simulation are shown in Figures 4c and 4d.

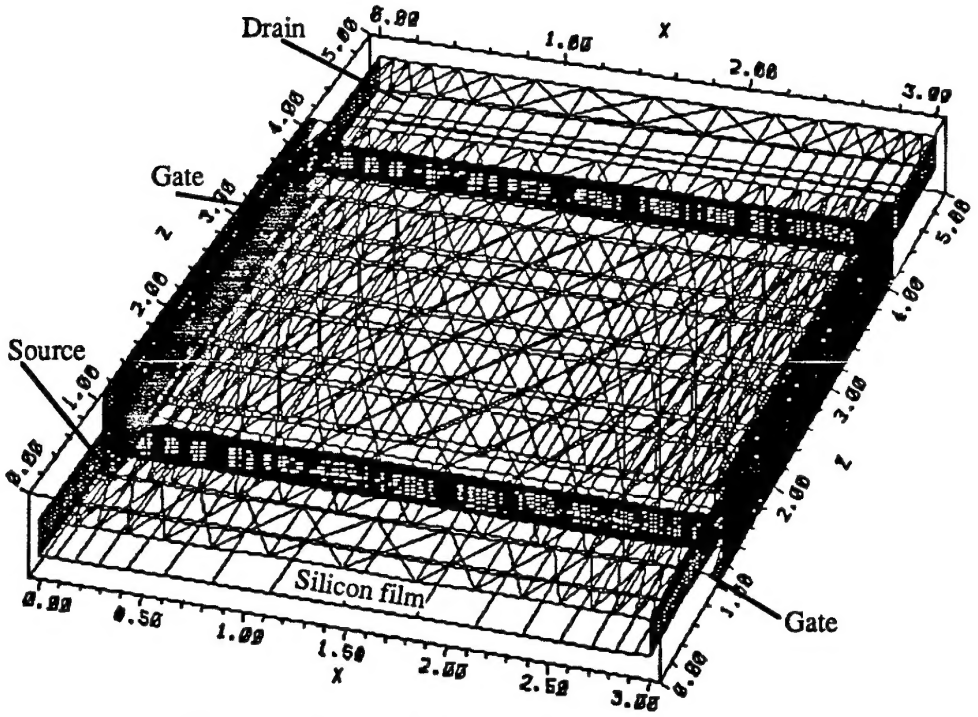

Figure 4c: 3D simulation mesh for the GAA device

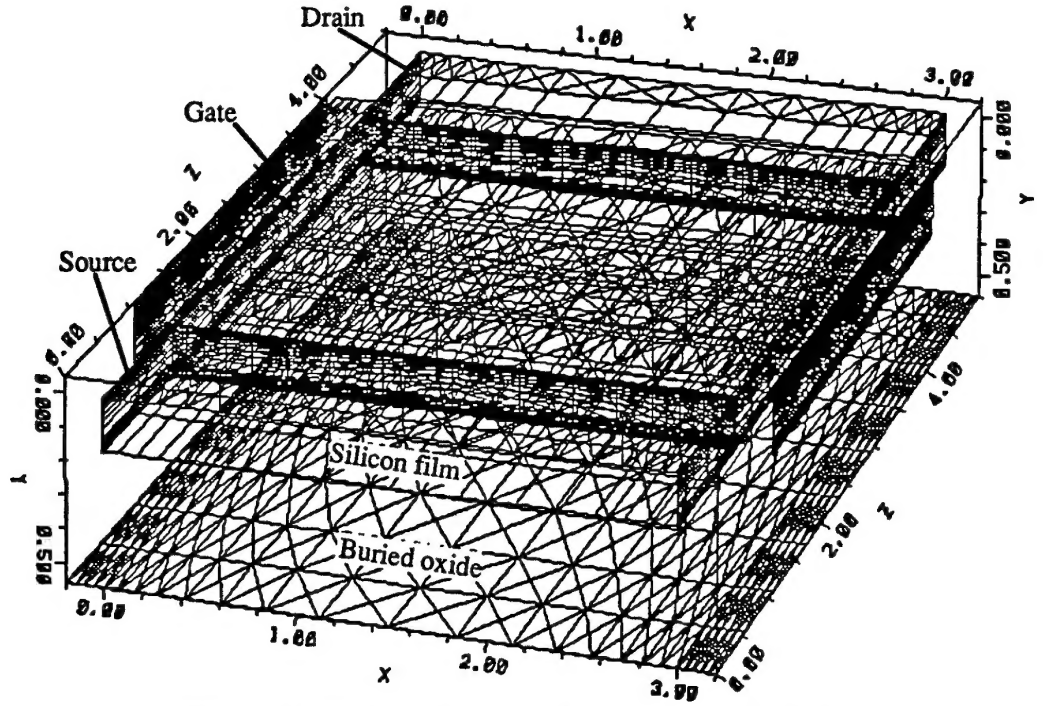

Figure 4d: 3D simulation mesh for the regular SOI device

$I_D(V_G)$ curves were simulated at V_{DS}=50 mV for various charge densities at the Si/SiO_2 interfaces: 10^{10}(pre-rad), $5x10^{11}$, 10^{12}, and $1.5x10^{12}$ cm^{-2}. These represent the charges generated in the oxides by arbitrary radiation doses. The $1.5x10^{12}$ cm^{-2} density

corresponds approximately to a dose of 500 krad in our case. In this simulation, uniform densities of charges were used across the structures. This is realistic for GAA devices, where all the oxide in contact with the active silicon is gate oxide, but it represents a best-case condition for the regular SOI device, where buried and sidewall oxides are of lesser quality than the gate oxide and, therefore, have a higher hole trapping factor. These simulations will thus compare the GAA devices and regular SOI devices with "ideal" lateral isolation oxides. Figure 5 presents the logarithmic $I_D(V_D)$ curves produced by the simulation. The kink in the pre-rad GAA transistor is clearly visible, and a slight kink can be observed in the regular SOI device as well.

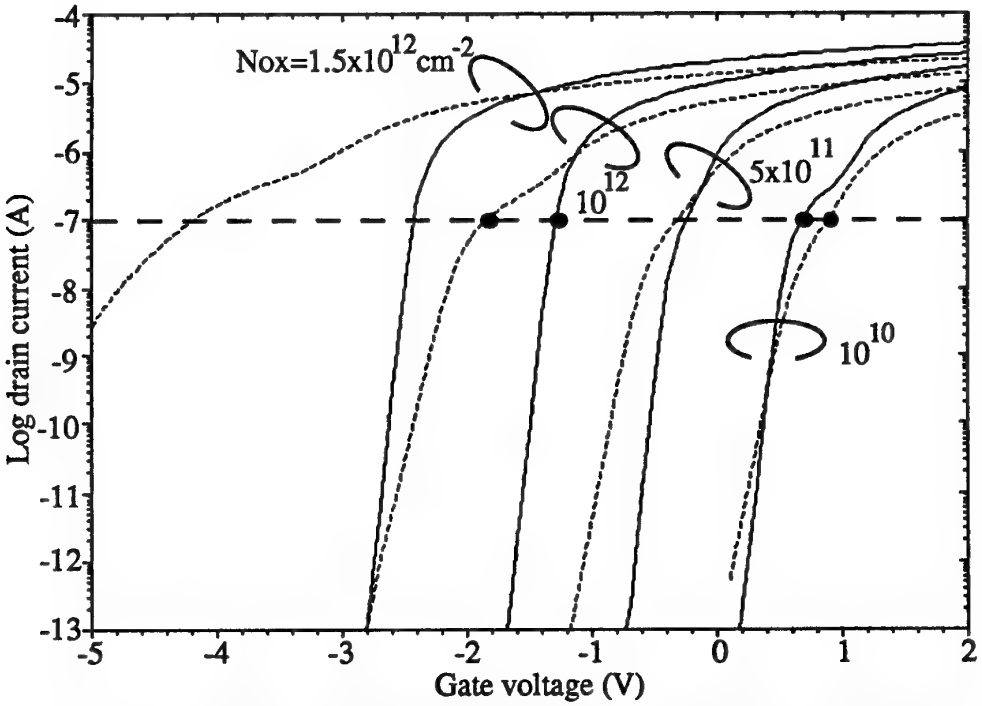

Figure 5: Simulated log $I_D(V_G)$ curves of an n-channel GAA device (solid lines) and a regular SOI MOSFET (dotted lines) with different oxide charge densities. The horizontal dotted line and the black dots correspond to the current level and the bias points used in Figures 7 to 10.

Upon increased dose irradiation (when the oxide charge density is increased), the kink tends to disappear in the GAA device, while it gets more and more pronounced in the SOI transistor. The same curves are presented on a linear scale in Figure 6.

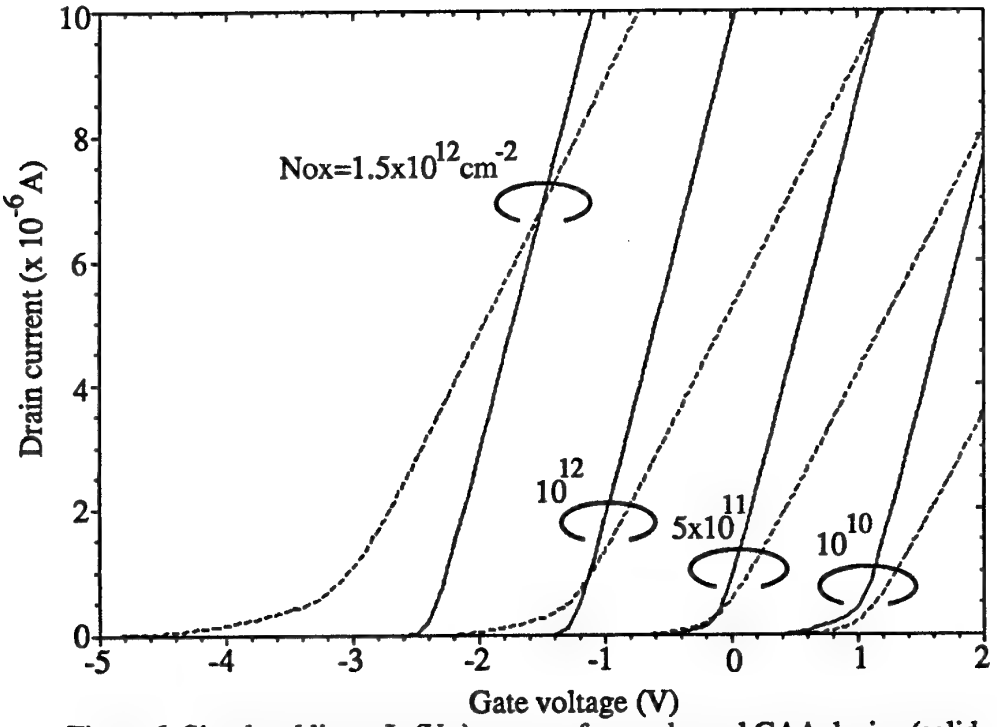

Figure 6: Simulated linear $I_D(V_G)$ curves of an n-channel GAA device (solid lines) and a regular SOI MOSFET (dotted lines) with different oxide charge densities.

Understanding of this effect can be gained by examining 2D contour plots of the electron concentration in cross-sections of the devices in the middle of the channel region. These cross sections are taken for a drain current of 10^{-7} A, *i.e.*, right below the kink in the curves of Figure 5. Figure 7 presents electron concentration contours in the regular SOI device before irradiation, *i.e.* with an oxide charge density of $10^{10}cm^{-2}$ (gate voltage = 0.88 V).

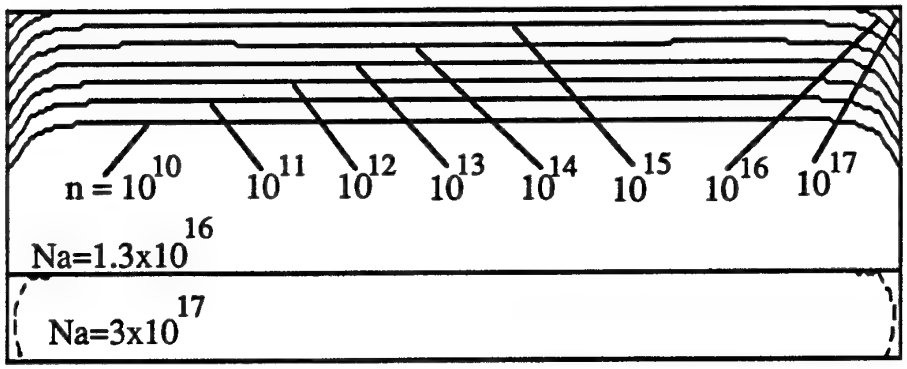

Figure 7: Electron contour plots in a cross section perpendicular to the current flow direction in the regular SOI MOSFET before irradiation (oxide charge density = $10^{10}\,cm^{-2}$, gate voltage = 0.88 V, $I_D = 10^{-7}$ A).

Figure 8 presents electron concentration contours in the same device after irradiation, (oxide charge density $=10^{12}cm^{-2}$, gate voltage = -1.84 V). It can be clearly seen that in

the unirradiated device current flows mostly in the top channel, while edge leakage is the main factor of current conduction in the irradiated transistor. The results are totally different if the same simulation is conducted for GAA devices.

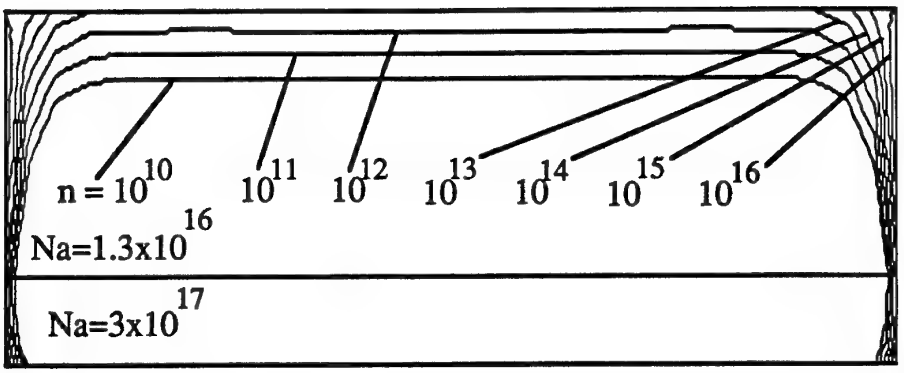

Figure 8: Electron contour plots in a cross section perpendicular to the current flow direction in the regular SOI MOSFET after irradiation (oxide charge density = 10^{12} cm^{-2}, gate voltage = -1.84 V, $I_D = 10^{-7}$ A).

Figure 9 presents electron concentration contours in the GAA device before irradiation, *i.e.* with an oxide charge density of $10^{10}cm^{-2}$ (gate voltage = 0.7 V). It can be seen that most of the current flows along the edges of the device, causing the kink in the subthreshold characteristics.

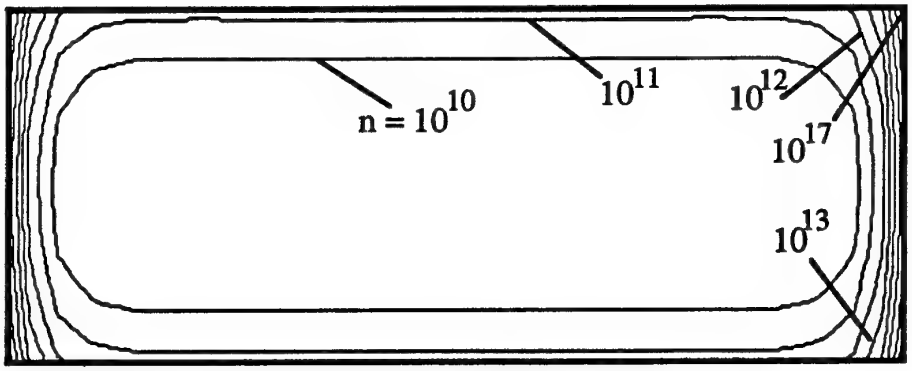

Figure 9: Electron contour plots in a cross section perpendicular to the current flow direction in the GAA device before irradiation (oxide charge density = 10^{10} cm^{-2}, gate voltage = 0.7 V, $I_D = 10^{-7}$ A).

After irradiation, however, the edge electron concentration is equal to that at the top and bottom of the silicon film (Figure 10, gate voltage = -1.3 V, oxide charge density = 10^{12} cm^{-2}), such that the current flowing along the edge of the device is no longer visible on the $I_D(V_G)$ characteristics (the lateral threshold voltage is equal to the main transistor threshold voltage).

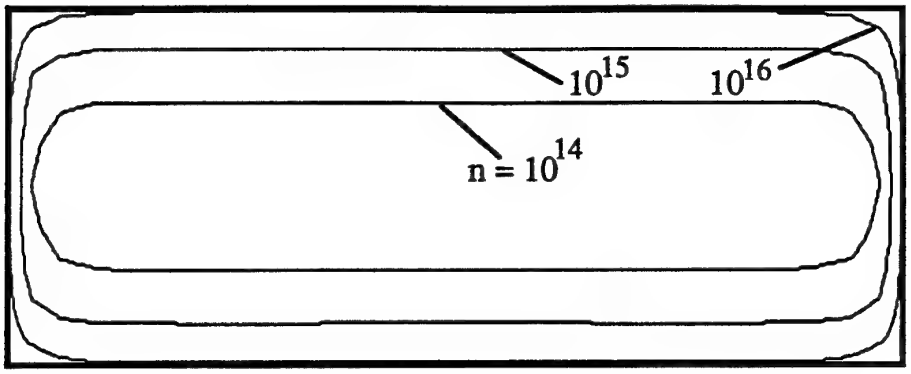

Figure 10: Electron contour plots in a cross section perpendicular to the current flow direction in the GAA device after irradiation (oxide charge density = 10^{12} cm^{-2}, gate voltage = -1.3 V, $I_D = 10^{-7}$ A).

The physical explanation for the presence of an edge leakage current in the unirradiated SOI device can be found in [11]: the depletion charge in the silicon film near the edges of the device is shared between the front Si-SiO_2 interface, the back Si-SiO_2 interface and the edge Si-SiO_2 interface. As a result, the local threshold voltage is lowered with respect to that of the regular front interface. After irradiation, all threshold voltages are shifted to lower values by the presence of positive oxide charges. Under the assumption of constant charge density distribution in the oxides this variation is proportional to the thickness of the oxide layers and the threshold shift is largest for the lateral gate in the regular SOI MOSFET. In other words, the control of the electron concentration at the edge of the device is weak because of the relatively thick gate oxide. Indeed, as can be seen in Figure 11 (oxide charge density = 10^{12} cm^{-2}) the presence of a negative gate voltage (-1.84 V) generates a weaker electron-repelling electric field along the edges of the device than in the corners or the main (top) Si-SiO_2 interface. As a result, an edge leakage current is observed.

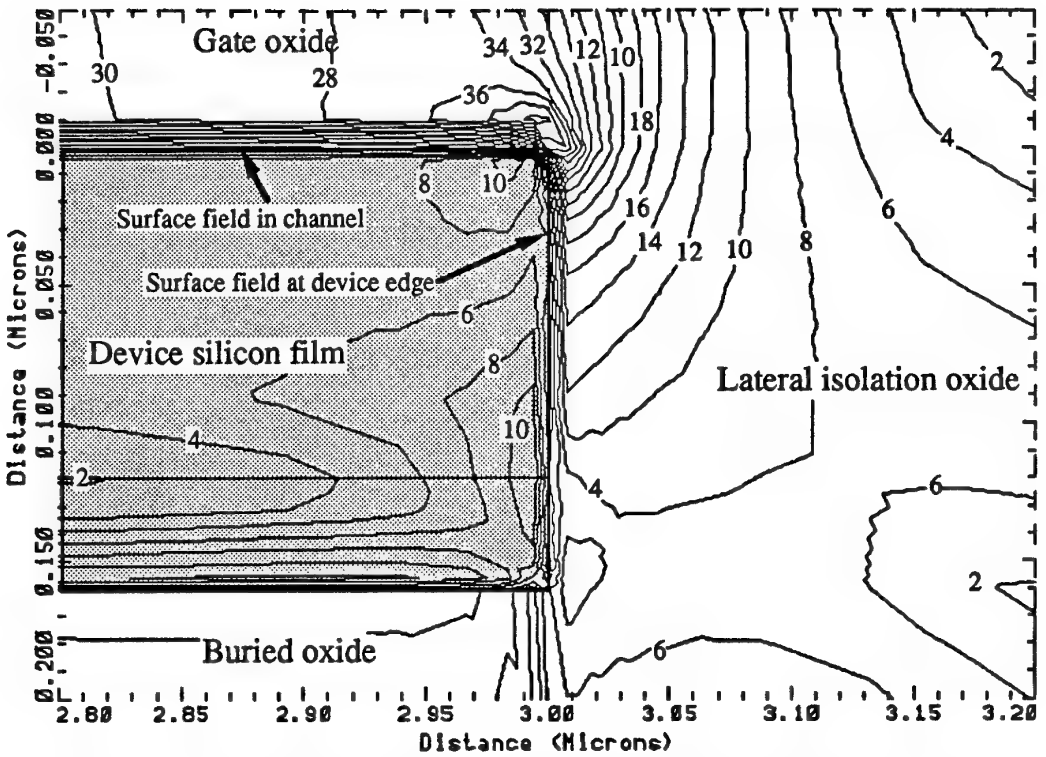

Figure 11: Constant electric field contour plot (x 10^4 V/cm) at the right edge of the regular SOI MOSFET after irradiation (oxide charge density = 10^{12} cm^{-2}, gate voltage = -1.84 V). The values of the electric field in the SiO_2 at the Si/SiO_2 interfaces are $12x10^4$, $4x10^4$ and $28x10^4$ V/cm in the main channel, at the device edge, and in the top corner, respectively.

In the case of the GAA device, the control of the electron concentration by the gate at the edges of the device is largely improved. This is not only due to the presence of a thinner lateral oxide, but also to a two-dimensional effect similar to the "tip effect". Indeed, the potential difference between the gate voltage (V_G = -1.3 V) and the device silicon film gives rise to a large electric field at the corners of the device. The gate being at a more negative potential than the silicon film, this high electric field tends to repel electrons and to locally enhance the threshold voltage (with respect to the main channel threshold voltage). This effect is illustrated in Figure 12 (oxide charge density = 10^{12} cm^{-2}, gate voltage = -1.3 V, $I_D = 10^{-7}$ A), where the contours of iso-electric field lines are plotted in the vicinity of the edge of the device.

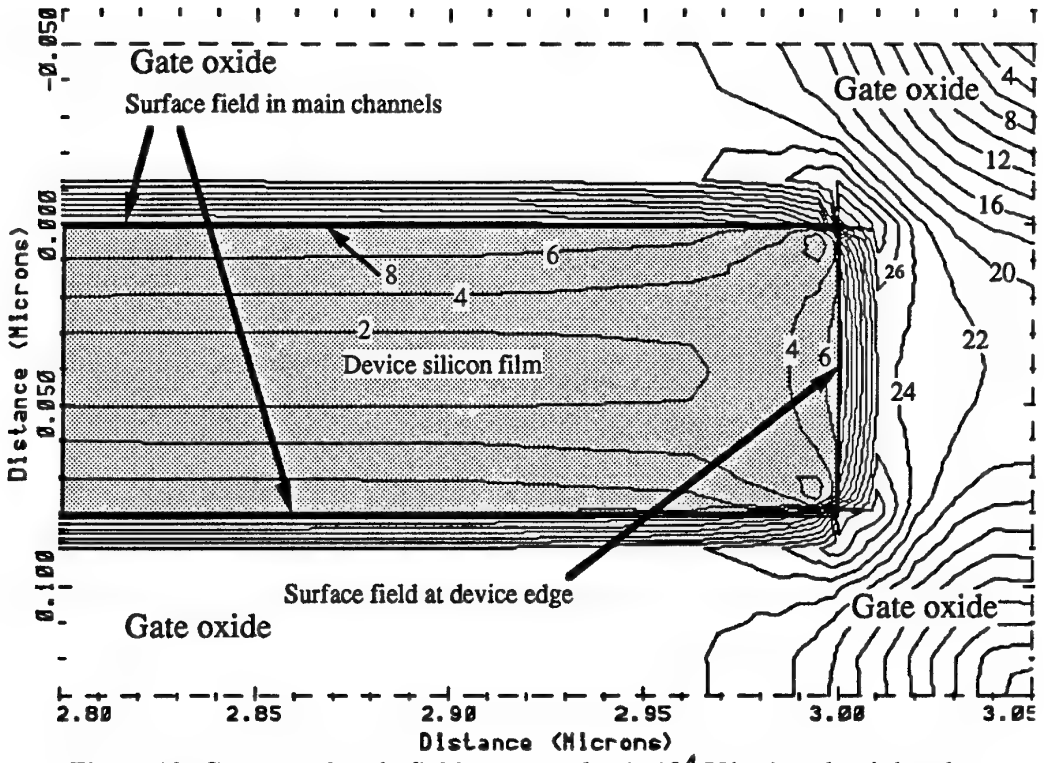

Figure 12: Constant electric field contour plot (x 10^4 V/cm) at the right edge of the GAA device after irradiation (oxide charge density = 10^{12} cm^{-2}, gate voltage = -1.3 V). The values of the electric field in the SiO_2 at the Si/SiO_2 interfaces are $8x10^4$, $9x10^4$ and $18x10^4$ V/cm in the main channels, at the device edge, and in the corners, respectively.

The electron-repelling surface electric field value is $8x10^4$ V/cm in the main channel regions, while it reaches higher values on the lateral edge of the device, and in the corners. In a GAA device, when the gate voltage is more positive than the surface potential (which is the case at threshold before irradiation), the tip effect tends to increase the electric field and the potential at the corners, which increases the edge leakage current. Upon irradiation, as the gate voltage is lowered to keep the same drain current level (10^{-7} A in our case), the tip effect is reduced. Eventually, for larger irradiation doses, the gate voltage has to become more negative than the surface potential to maintain the same drain current level. In that case, the tip effect increases again, this time decreasing the electron concentration at the edges. This explains the disappearance of the kink in the $I_D(V_G)$ curves of the GAA device upon irradiation.

Let us now take a line at the surface of the silicon (right below the gate oxide located at the top of the device. Let this line run from the center of the device to its edge (*i.e.* from y=W/2 to y=W). The Figure below presents the electron concentration along this line for a constant current ($I_D = 10^{-7}$ A) and for two different gate oxide charge concentrations (Qox = 0 and $5x10^{11}$ cm^{-2}). These two charge densities represent pre-rad and post-rad conditions, respectively (Figure 13).

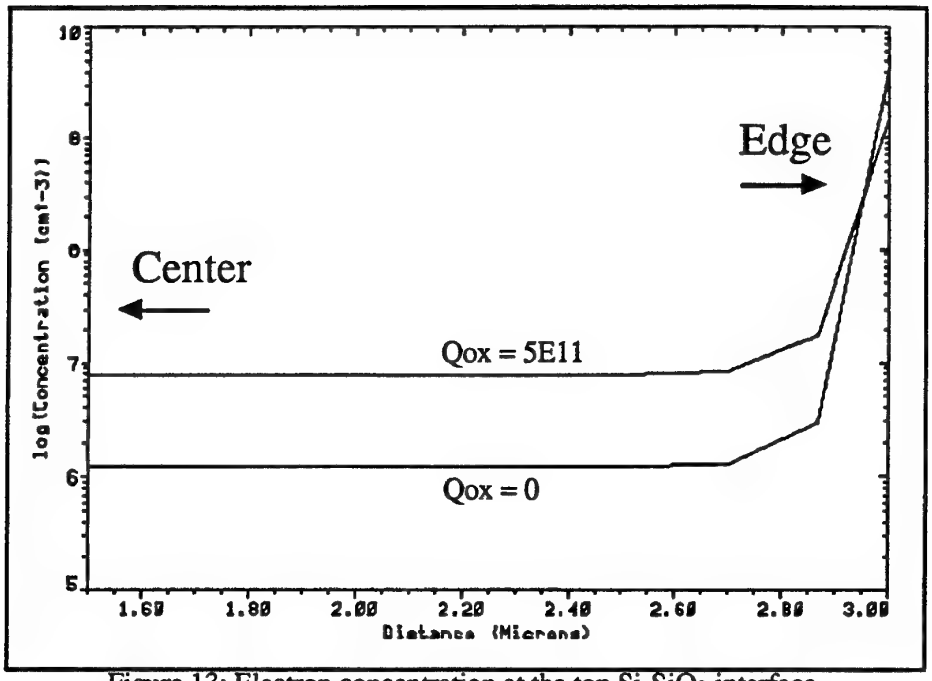

Figure 13: Electron concentration at the top Si-SiO_2 interface

One can notice that, although the overall current flowing through the device is the same, more current transport takes place at the edges of the device in the pre-rad case than in the post-rad one, thereby indicating that the lateral threshold voltage shifts less than the main transistor's threshold voltage upon irradiation. This behaviour is particular to GAA devices and is opposite to that found in regular SOI devices.

2.1.5. Conclusions

Ordinary SOI n-channel transistors show an increase of edge leakage current upon dose irradiation due to the larger threshold voltage shift at the edge of the devices than in the main transistor. The opposite behaviour is observed in gate-all-around transistors: the threshold voltage at the edges of the device shifts less than that of the main transistor upon creation of oxide charges due to the exposure to radiations. This effect has been observed experimentally and is explained by device simulation.

2.1.6. References

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3. Design

3.1. GAA HSPICE parameters

The parameters introduced in the hspice level 3 model for GAA circuit design are the following:

for the pMOS transistor:

vt0=-0.738	phi=111.61	gamma=0.001	nsub=1e11
nfs=7.5e10	u0=458.74	vmax=563890	xj=5e-08
ld=5e-07	theta=0.08038	tox=5.5e-08	wd=2e-07
is=0	js=0	jsw=0	cj=0
cjsw=0	mj=0	mjsw=0	rsh=243
delta=0	kappa=9.5	eta=0.0027873	acm=0

for the nMOS transistor:

vt0=0.692	phi=119.0496	gamma=0.053479	nsub=5.859e21
nfs=3e+12	u0=911.5368	vmax=5e+07	xj=1.37e-06
ld=4e-07	theta=0.119753	tox=5.5e-08	wd=2e-07
is=0	js=0	jsw=0	cj=0
cjsw=0	mj=0	mjsw=0	rsh=243.24
delta=0	kappa=0.01	eta=0.156324	acm=0

Those parameters were obtained by fitting simulation current curves on experimental data measured on n and p minimum size transistors (3x3µm). Id-Vg curves in the linear regime (Vd=+/-0,05V) and Id-Vd curves were both considered with Vg and Vd going from 0 to 3V maximum.

****

Simulations of the total dose effect were performed with initial values of the threshold voltage equal to 1V for n channel transistors and -0,5V for p channel devices. We further assume that the shift rate of n type transistors is 4 times greater than for pMOS devices. Finally, $\Delta V_{t,n}$ is swept from 0 to 4V by steps of 0.1V.

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3.2. GAA memory circuits

3.2.1. Introduction

This Section describes design considerations for a static random access memory submitted to ionizing irradiation. First we recall that in a static memory, the data is stored in latches, while dynamic memory gates store their data on capacitors. The static memory cell has a non-destructive readout and retains its data under application of the dc supply voltage. On the other hand, the dynamic cell has a destructive readout and needs the application of a periodic refresh. Static memory is therefore inherently more robust against irradiation than dynamic storage.

We will concentrate on total dose radiation effects which mainly introduce a negative threshold voltage shift of both n- and p-channel transistors. We assume that other effects such as an increased leakage current and a reduced mobility can be suitably overcome by adequate processing during the device fabrication and stay within acceptable limits. The design of radiation hard circuits can therefore be reduced to the design of a threshold voltage variation inert circuit. It is known that the V_t shift has a close relationship to the polarity of the gate bias under irradiation. The V_t shift becomes larger when the bias is positive because the Si/SiO_2 interface trap centers will capture more positive charges, rejected by the gate. Thus, in general operating conditions we may expect $\Delta V_{t,n}$ to be larger than $\Delta V_{t,p}$, and we have quite arbitrarily chosen $\Delta V_{t,n} = 4\ \Delta V_{t,p}$. This hypothesis relies on the fact that the gate-to-source or gate-to-drain voltage reaches a maximum of 5V for n-channel transistors and 0V for p-channel transistors when they are 'on'. The opposite conclusion arises nevertheless when they are 'off'.

Gate-All-Around (GAA) devices are expected to be relatively radiation hard because the silicon film is only in contact with a very thin, thermally grown gate oxide. The threshold voltage shift is consequently reduced under irradiation (electrical influence of t_{ox}^2 in V_t). But one major drawback of this technology is the only possibility of producing minimal size transistors. Indeed, the silicon bridge between source and drain breaks if the transistor is too large or too wide. So, only 3µm x 3µm square transistors are available. If a width to length (W/L) ratio less (greater) than unity is required, several separated minimal transistors have to be placed in series (in parallel). Therefore, the GAA design rules do not allow very compact layouts compared to conventional SOI.

A memory consists of several basic blocks including column and row decoders, read and write circuits and an array of memory cells.The implemented architecture introduces a strong redundancy of different circuits to increase the reliability at the expense of a greater circuit area. The realization in a near future of an 1K bit memory will require to be careful to the surface compactness.

The global architecture may be described as following (Fig.1): memory cells are arranged in an array of 8 x 8 bits with 8 pairs of access buses (bit lines) running horizontally (rows), and 8 select lines (word lines) running vertically (columns). Eight write circuits, one for each pair of buses, are connected on the left of the array and 8 read circuits are connected on the right. Only one read and one write circuit are normally active at a time. Eight of them are present to study various designs and meet the redundancy purpose. Two decoders perform the vertical and horizontal selection of only one cell, one read and one write circuit for each operation. The input is common for all write circuits and there is only one three-stage output buffer following all read circuits.

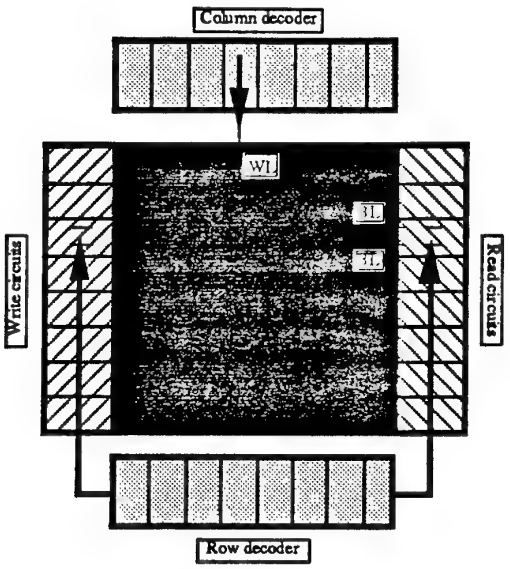


Figure 1: Global architecture of the implemented memory.

The goal is to choose the appropriate W/L ratio of each transistor so that the write operation (switching of the cell internal state) as well as the read operation (holding of the cell internal state) is possible in a wide range of threshold voltage variation.

3.2.2. Memory cells

A memory cell is mainly a flip-flop formed by two storage nMOS transistors and two load elements. These may be either load resistors, enhancement or depletion mode nMOS transistors or pMOS transistors. The latter full CMOS static solution provides a lower standby power dissipation because no current flows through the cell except when it is switching. It also increases the noise margin between the high and low state due to continuous restoring of the information. The drawback is a larger memory size. Two access transistors, generally nMOS, connect the cell to a pair of bit lines. We will demonstrate the usefulness of implementing p-channel select transistors although this carries an area penalty due to the reduced driving capability of p-channel devices. The single-ended five-transistor static CMOS cell could be used to reduce the circuit area but the non-differential read and write operations diminish the robustness against threshold voltage variations. In the compromise between performance and cost, we deliberately favour high performances.

Information is stored in the form of voltage levels in the two cross-coupled inverters. The two stable states can be designated '1' (achieved with 'int_g' high and 'int_d' low: T_1, T_4 off and T_2, T_3 on) and '0' (achieved with 'int_g' low and 'int_d' high: T_1, T_4 on and T_2, T_3 off) (Fig.2).

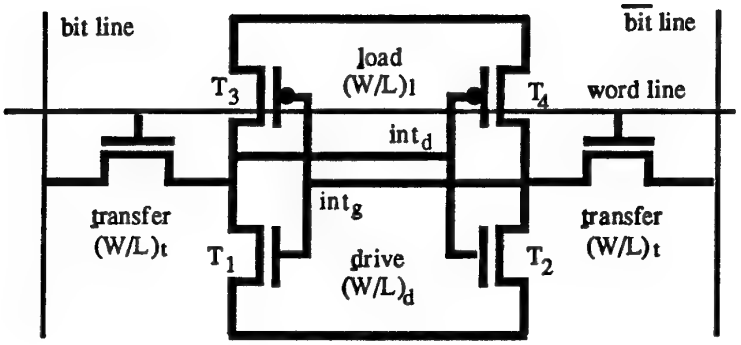


Figure 2: The memory cell.

The cell design is performed as follows. Firstly, we fix the width to length ratio $(W/L)_d$ of the of n-channel drive transistor of each inverter. This parameter choice relies on a tradeoff between memory speed and limitation of the cell size. We have adopted $(W/L)_d = 2$ which implies the use of two minimal GAA transistors in parallel. Then, two parameters are further involved in the cell design: the width to length ratio $(W/L)_t$ of the transfer device which yields the cell ratio (ratio of $(W/L)_d$ to $(W/L)_t$) and the width to length ratio $(W/L)_l$ of the load transistor. In order to benefit from a sufficient noise margin in the read operation, a high $(W/L)_l$ is desirable. On the other hand, the write operation becomes more and more difficult if $(W/L)_l$ increases. The same incompatible requirement affects the transfer gate: when $(W/L)_t$ is too small, the voltage drop across the access device is too large and the writing operation fails. When $(W/L)_t$ is too large, too much current will dump into the cell during the read operation, inducing a switching of the internal state. Here we can feel the importance of the select transistor type: as the threshold voltage shift is always negative under irradiation, n-channel transistors become less resistive and therefore facilitate the write operation to the prejudice of the read operation. The opposite situation occurs with a p-channel select transistor.

So, the cell optimization is inherently difficult as the requirements induced by the two main operations may be incompatible.

In our memory prototype, we have implemented different cells with $(W/L)_l$ varying from 3 to 10. $(W/L)_t = 3$ or 4 if a n-channel transfer gate is used and $(W/L)_t = 4$ or 8, in the case of a p-channel access device (Fig.3).

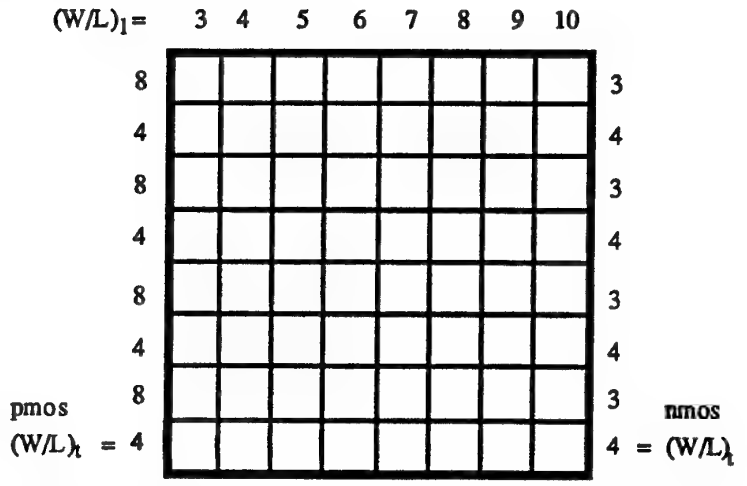


Figure 3: Parameter variation in the memory prototype.

3.2.3. The write circuit

The write circuitry is relatively straightforward. It typically consists of two cascaded inverters followed by a pass gate with a write control input signal to the bit and $\overline{bit}$ lines. This pass gate may be either an n-channel device, a p-channel transistor or a three-state clocked gate (Fig.4). In the latter case, the clocked transistors directly surround the output in order to avoid a capacitive coupling between the input node and the output bit or $\overline{bit}$ lines (clk). (In the isolation state, the output is then independent of any variation of the input logic level). When the clocked transistors are in the 'on' mode, the gate behaves like a simple inverter. Its static transfer curve is very similar to the characteristic of an inverter with the same global ratios $(W/L)_p$ and $(W/L)_n$.

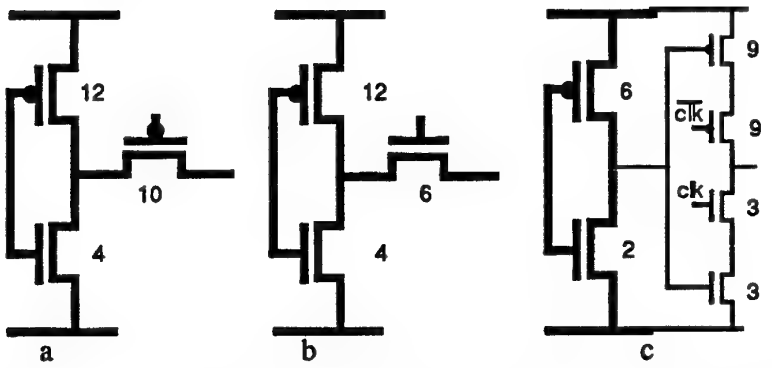


Figure 4: The write circuit: a) with a p-channel pass transistor; b) with a n-channel pass transistor; c) with a three-state pass gate.

We must provide the inverters with a sufficient drive capability and pass gates with a sufficient low resistance so that they can deliver enough current to switch the cell internal state.

Under irradiation, the transfer characteristic of the inverters shifts left, and the high logic level is degraded. The major concern is nevertheless the modification of the isolation provided by the pass gate. A direct consequence of the irradiation is that the threshold voltage of n-channel transistors decreases and becomes negative. At this moment, the n-channel pass transistor is impossible to turn off and the isolation between the write inverters and the bit and $\overline{bit}$ lines may no longer be ensured. If we choose a p-channel pass transistor, it becomes more resistive under irradiation implying a more and more difficult write operation Finally, the three-state gate also brings its disadvantage under irradiation: the nMOS transistors, always in the on state, tends to impose a low output voltage on both bit and $\overline{bit}$ lines which opposes to the normal precharge and read operations.

The threshold voltage shift obtained during irradiation is strongly influenced by the gate-to-substrate V_{gb} bias under irradiation. In SOI, the silicon film is floating and the body potential is considered to be equal to the source potential. Therefore, we consider V_{gs} rather than V_{gb}. The higher V_{gs} or V_{gd}, the larger the threshold voltage shift. We assume that the pass gate is in the off state under irradiation because the memory is in standby. Consequently, if we consider that all pass gate are 'off' during irradiation, the most critical gate-to-source bias is $V_{gs}=V_{dd}$ for p-channel access transistors (V_g=5V, V_s=0V) and V_{gs}=0V for n-channel select transistors (V_g=0V, V_s=0V). For the three-state gate, the worst case bias is $V_{gd}=V_{dd}$ for n-channel

transistors (V_g=5V, V_s=0V) and $V_{gd}=V_{dd}/2$ for p-channel transistors (V_g=5V, V_s=2.5V) because the voltage at the intermediate node is about $V_{dd}/2$ (Fig.5). Considering p-channel devices, the three-state gate configuration is therefore preferable to the pass transistor. But we must conclude the opposite for n-channel devices.

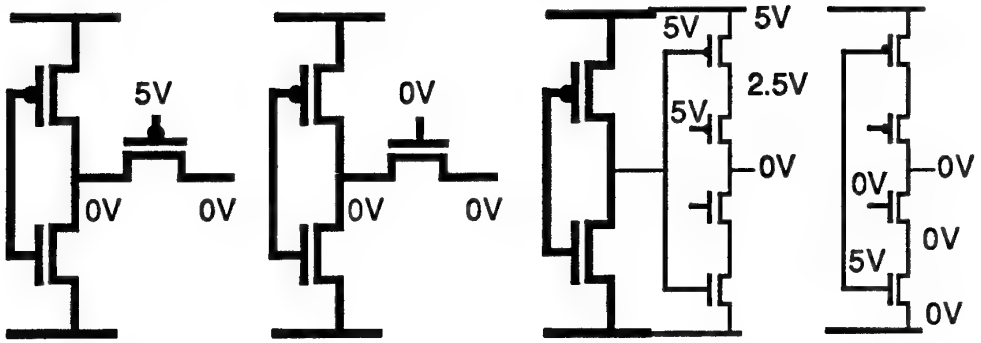


Figure 5: Worst case bias of the different pass gate under irradiation.

To perform a complete study of these various influences, our test circuit contains write cells with different types of pass gate: n-channel transistor and three-state gate if the memory cell access transistor is n-type; p-channel transistors and three-state gate for p-type memory cell access devices. The write circuits are also implemented separately.

3.2.4. The read circuit

The read circuit is more complex since it involves the use of a sense differential amplifier. It must be able to sense and amplify a very small difference between the levels on the bit and $\overline{bit}$ lines. We used the simple single ended pMOS differential amplifier shown in Figure 6.

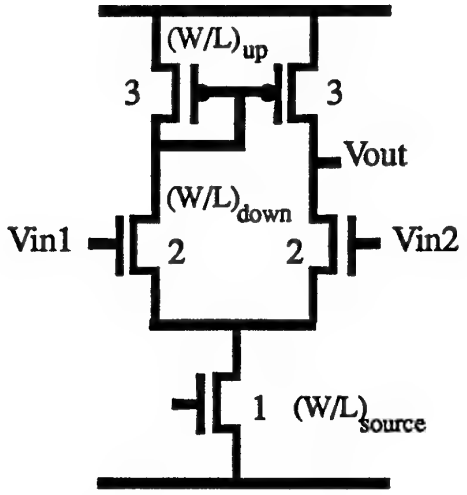


Figure 6: The differential sense amplifier .

The design goal essentially consists in creating a circuit which symmetrically reacts to the inputs. Ideally we must obtain:

$0V < V_{out} < 2.5V$ for $V_{in1} < V_{in2}$,

$2.5V < V_{out} < 5V$ for $V_{in1} > V_{in2}$

and $V_{out} = 2.5V$, for $V_{in1} = V_{in2}$.

More generally, when $V_{in1} = V_{in2}$, the output voltage of the read circuit (V_{out}), must be equal to the switching point of the output buffer that follows. This is clearly not possible for all values of $V_{in1} = V_{in2}$. The greatest sensibility to the variation of the parameters is obtained with $V_{in1} = V_{in2} = 5V$. Therefore, this bias will be used as standard calibration of the sense amplifier.

Under irradiation, the switching point shifts negatively by a large quantity (2V for DV_t =-4V). V_{out} also shifts negatively due to the reduced and increased driving capability of n- and p-channel devices respectively. This shift is unfortunately less pronounced than the buffer switching point shift (0.5V for DV_t= -4V). Therefore, the equality may not be maintained through the whole range of threshold voltage variation. What we can do is to start with V_{out} when $V_{in1} = V_{in2} = 5V$ slightly smaller than the switching point of the inverters (about 3V) before irradiation. V_{out} will become greater than the switching point when the radiation dose increases.

The read circuit is not very sensitive to the different parameters. Let $(W/L)_{down}$ be the width to length ratio of the nMOS differential input pair and $(W/L)_{up}$ be the same ratio for the pMOS current mirror. V_{out} does not vary as a function of $(W/L)_{down}$ as soon as $(W/L)_{down}$ exceeds 3 and is slightly higher when $(W/L)_{down}=2$. We have chosen, quite arbitrary, this last value. On the other hand, V_{out} increases as a function of $(W/L)_{up}$ and tends to saturate for $(W/L)_{up}$ greater than 6. We have adopted $(W/L)_{up} = 3$ which gives an initial value of V_{out} when $V_{in1} = V_{in2} = 5V$ quite small, equal to 2,75V. This choice relies in a tradeoff between the lack of balance allowed before irradiation and the performance achieved after irradiation. It is also worth to note that we have adopted $(W/L)_{source}=1$.

3.2.5. The output buffer

The function of the output buffer is obvious. It aims to isolate the output node of the read circuit from the relatively heavy output load capacitance (plot capacitance ≅ 1pF and scope input capacitance ≅ 15pF). It consists of a chain of inverters, getting larger as one reaches the output. The first inverter of the chain has to be small, in order to present a negligible gate capacitance to the read circuit. The last inverter of the chain must have the driving ability to charge and discharge the output node without limiting the operational frequency of the memory. In the middle of the chain, each inverter is chosen so that it can drive enough current to charge and discharge the gate capacitance of the following inverter, while presenting a reasonable low gate capacitance to the previous inverter in the chain. The ideal ratio between the number of nMOS transistors in these inverters is close to $1:n:n^2:n^3$ ... (Fig.7). We have adopted n = 3.

If n is increased, the output curve follows the input with a longer delay, essentially due to the charge and discharge of a greater gate capacitance by the first inverter, but the curve exhibits a steepest slope. The maximum of the slope is achieved for n = 6, beyond this value, only the delay is increased. The optimum value for n is therefore somewhere between n = 3 and n = 6.

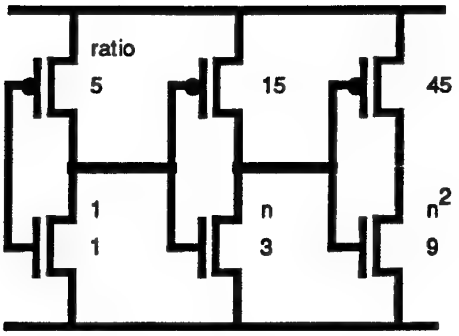


Figure 7: The output buffer.

The transfer characteristic of the inverters unfortunately shifts left under irradiation due to the negative nMOS and pMOS threshold voltage shift. Moreover, the high output level is very difficult to maintain and is often very degraded even at zero input bias because we eventually no longer can reach the off state of the n-channel transistors ($V_{t,n} < 0$).

The transfer characteristic shift is about the same for any ratio between the number of n and p-channel transistors. But if the switching point is initially placed beyond 2.5V (if $m_p\ (W/L)_p > m_n\ (W/L)_n$), the inverter will resist to a greater left shift induced by the irradiation. With 3 p-channel transistors for 1 n-channel transistor, the switching point of the transfer characteristic is localized at 2.95V in normal conditions and shifts to 0.9V for ΔV_t= -4V. With a ratio of 4 transistors pMOS for 1 transistor nMOS, the switching point starts at 3.1V and becomes 1.1V after the same irradiation. Fig ... shows the switching point evolution as a function of the threshold voltage shift ($\Delta V_{t,n} = \Delta V_{t,p}*4$).

We have chosen a ratio of 5 transistors pMOS for 1 transistor nMOS. Simulations show that the initial switching point is 3.2V and becomes 1.8V for ΔV_t= -4V. The high output level is still 4.5V after irradiation. A ratio of 3 would have given a switching point at 3V becoming 1.2V after irradiation and a high logic level decreasing to 4.1V.

With 3 stages and a capacitive load of 2pF, the maximum frequency achieved is higher than 100MHz. The last stage already requires 45 p-channel transistors. An additional stage would necessitate 135 p-type transistors and would be extremely area consuming. Therefore, we limit our buffer to 3 stages and we will eventually have recourse to an external amplifier in the follower configuration to limit the output capacitive load at about 2pF.

3.2.6. The decoders

A column decoder is necessary to select one word line out of a set of columns in the array. This decoder controls the cell access gates. It must provide "one output high and all the others low" if the select transistor is n-channel type, "one output low and all the others high" for a p-channel access device. We must also be able to disconnect all the cells from bit and $\overline{bit}$ lines in order to properly precharge the buses for example. Therefore, the decoder must also be designed to yield "all outputs low" or "all outputs high" according to the chosen cell select gate.

A row decoder selects the desired bit pairs out of the row set in the array. In fact, this decoder only controls the write and read circuits. One of the read circuits is permanently active, which designates the active bit pair. The corresponding write circuit is either active (write operation) or not (read operation). The row decoder must therefore

provide the control command of the write circuit ("one output high and the others low", "one output low and the others high", "all outputs low", "all outputs high" or both commands) according to the pass gate adopted (p-channel, n-channel transistor or three-state gate). It must also provide the control sequence of the read circuit which is simpler (always "one output high and the others low'") because it invariably commands n-channel source transistor of the differential sense amplifiers.

Decoders can be realized in the full static CMOS technology. To control n-channel transistors, the decoder consists of a NOR gate fed by the address bits. This gives the selection signal "all '0' and one '1' ". A AND gate follows to introduce the clock enable function. The sequence becomes either " all '0' " or stays "all' 0' and one '1' " (Fig.8).

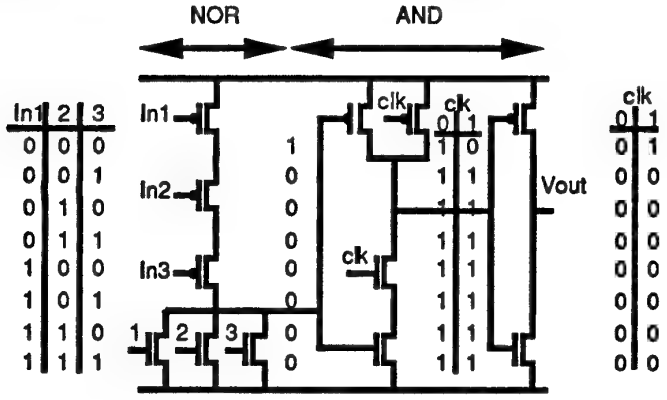


Figure 8: Decoder based on a NOR gate.

But NOR gates are inherently slow because pMOS transistors are in series. After irradiation, the poor driving capability of p-channel devices will be further reduced, while the high logic level will be strongly degraded due leakage currents of n-channel transistors. The NAND design where the nMOS transistors are in series is much more robust to the threshold voltage shift induced by the irradiation. Therefore, we will replace the NOR gate by a AND gate to produce the sequence " all '0' and one '1' ". The final design is depicted in figure 9.

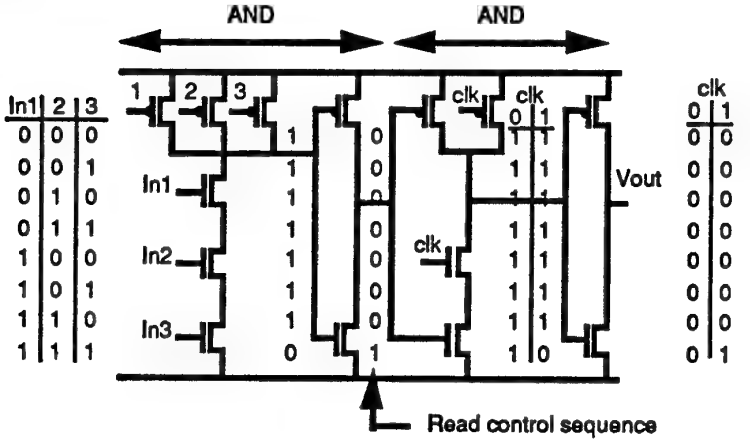


Figure 9: Decoder based on NAND gates only.

The robustness of this design is sufficient: the high logic level is still 4.3V for ΔV_t= -4V. The low logic level is of course not affected. With the same number of

transistors, the performances of the NOR gate would have been reduced : the high logic level falls to 1V as soon as ΔV_t= -2V.

To produce the opposite sequence " all '1' and one '0' " or " all '1' ", required to control p-channel transistors, we add an inverter to the previous design. We can not simply suppress the inverter of the last AND function because we need a sufficiently high driving ability to charge and discharge the word line capacitance. This capacitance is indeed large due to all the transfer gate capacitance connected to a word line. The performance of this new decoder is about the same: the high logic level is reduced to 4.1V when ΔV_t= -4V. The select signal of the read circuits must be independent of the enable clock and controls n-channel transistors. The required sequence " all '0' and one '1' " is already produced after the first AND gate of the decoder.

In order to reduce the circuit area when the number of input addresses increases, we may think to implement the decoders in a pure nMOS technology. The NOR function is then realized by n-channel devices in parallel, with a pMOS transistor load (Fig.10). As expected, this structure is far from robust against negative threshold voltage shifts. The high logic level drops to 0V as soon as ΔV_t is lower than -2V.

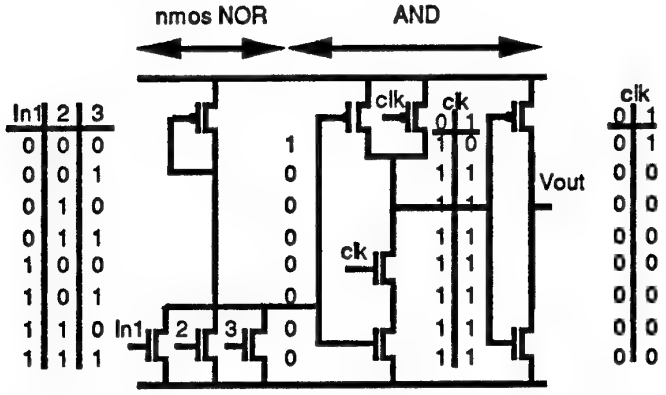


Figure 10: Decoder based on a NOR gate in the nMOS technology.

It is also possible to use dynamic decoders, where the NAND function is embed between two clocked transistors introducing the enable function. This gate is followed by a simple inverter (Fig.12). The design requires only a few transistors, but here again, the radiation hardness is poor. The gate tends to deliver the sequence "all ones" as soon as ΔV_t = -1.5V.

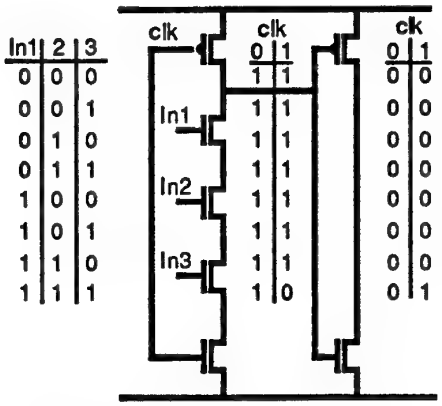


Figure 12: Dynamic decoder.

3.2.7. The write operation

In general, to write into the cell, data and $\overline{\text{data}}$ are placed on the bit and $\overline{\text{bit}}$ line respectively by allowing the correct write circuit to be connected to its bit line pair. Then one word line is activated. This will force the cell to flip into the state represented on the bit lines provided that the potential drop across the pass gate of the write circuit and across the cell access transistor is not too high.

3.2.8. The read operation

In general, the read operation is performed by starting with all the bit and $\overline{\text{bit}}$ lines high owing to the bit line load action. The column address input is decoded to select one of the word lines. All the cells along this word line are connected to their respective bit line pair. At this time, the data in the cell will pull one of the bit lines low. The row decoder then selects one of the 8 read circuits and hence one bit pair out of the 8 bit pairs available. The differential signal is detected on the bit and $\overline{\text{bit}}$ lines, amplified, and read out through the output buffer. Reading a static RAM is a non-destructive process and after the read operation, the logic state of the cell remains the same.

The bit line load is the impedance of a bit line to V_{dd}. It usually consists of a p-channel transistor with either its gate connected to its drain or its gate commanded by an external signal. In the first case, the load is full static and the pull-up operation is permanent. The precharge level is $(V_{dd}-|V_{t,p}|)$. This level will decrease when $V_{t,p}$ shifts negatively after irradiation. In the second case, the load is dynamic and the pull-up operation is limited in time. The precharge level is V_{dd}. With a full static load, a dc current flows from the bit line load to the ground through the accessed cell during the read or write operation. Therefore, the operating power of the memory is increased. The drawback of the dynamic load is that it requires an additional external signal which must be synchronized with the read operation. Moreover, a dynamic circuit implies a minimum operating frequency because the write operation has to occur before the bit lines are discharged by leakage currents. After irradiation this minimum operating frequency increases due higher leakage currents of n-channel transistors. But the maximum operating frequency decreases due to the reduced driving capability of p-channel transistors. Therefore, the performance degradation of dynamic circuits due to total dose effects may be more pronounced than the degradation affecting static circuits.

The advantage of the pull-up transistors is to precharge the bit lines and therefore speed up the access time. The read operation indeed requires the discharge of one bit line by a n-channel transistor and avoids the charge by a p-channel transistor (having a relatively poor driving capability, especially after irradiation). Another function of the pull-up transistor is to ensure the stability of the read operation. Let us define V_{FL} as the low bit line voltage at which the data changes from a high state to a low state in the cell when the voltage of the other bit line is kept at a high value. The precharge level of the bit line must be higher than V_{FL} to avoid a parasitic change of the cell internal state. A problem arises after irradiation, when the precharge level of static loads decreases.

The size of the dynamic pull-up transistor is quite large to speed up the precharge. We have chosen $(W/L)_{pull\text{-}up}=4$. The size of the full static pull-up transistors must be more reduced because the pull-up operation opposes to an easy discharge of the bit line by the low level side of the cell during the read operation. A strong pull-up load will also disturb the correct write operation of the low cell side. Therefore, we have adopted $(W/L)_{pull\text{-}up}=1/4$. After irradiation, the precharge operation slows down and the operating frequency increases.

In almost all cases, memory failure with radiation is due to leakage current which originates from n-channel devices operating in a depletion mode.

3.2.9. Address transition detection

Address Transition Detection (ATD) circuits are used to provide the initial pulse by which RAMs which are externally unclocked (asynchronous) can be operated as if internally clocked (synchronous). It is the original clock for subsequent internal clocks which control the timing for various internal operation. The address transition detection generates a one- shot pulse when one or more of the input signals such as addresses or enable functions have changed. In our simple case, we project to use this one-shot pulse to precharge the bit lines at V_{dd} before the read operation, when a dynamic pull-up load is implemented.

ATD can also provided equalization pulses when one or more equalization transistors are present in order to improve the access speed of the memory (equalization of the bit line voltages before the precharge, equalization of the two branch voltages of the differential sense amplifier which response is more rapid near the toggle point, ...). Equalization techniques have not yet been implemented. ATDs can also be involved in more complicated functions as the deselection of array sections to reduce the power consumption during the read and/or the write operation. Such improvements are out of the goal of this study.

The ATD is not yet integrated in our memory prototype but is investigated separately. The precharge signal, when required, must still be provided externally. The symbolic circuit diagram of the ATD we have chosen is shown in figure 13.

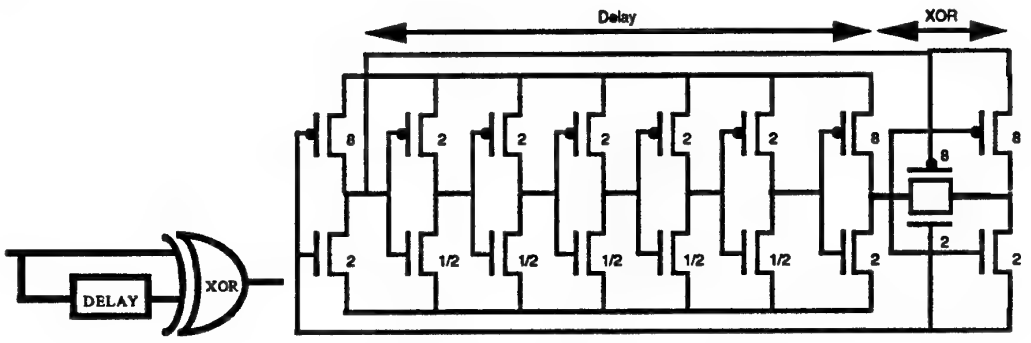


Figure 13: Address transition detection.

It essentially consists of an XOR gate and a DELAY block. The design is just a try without any particular radiation hardness design consideration. The DELAY block determines the one-shot pulse width and is realized by a chain of inverters. What about the evolution of the global response of this DELAY block when the p-channel drive capability decreases while the n-channel drive capability increases? The answer lies in the frequency response of a ring oscillator realized with the same inverters.

Simulations have revealed that the pulse duration is too short to be measured (10ns). More than five inverters are necessary in the delay block. But, by lack of space, we have introduced an artifact to increase the pulse duration. We have added an internal capacitance in the delay block. With an additional capacitance of 15pF, the pulse width is increased to 200ns. An output buffer isolates the ATD from the output capacitance load (15pF due to the scope). A pulse arises at each low to high or high to low address transition. The additional capacitance is charged by a p-channel transistor in the first case,

and is discharged by an n-channel transistor in the second case. After irradiation, the charge is slower and the discharge is a little bit faster. The switching of the next inverter, which determines the pulse width, however, arises at a lower gate voltage due to the left shift of the transfer characteristic.

Combining these two observations we observe that the switching level is reached earlier during the charge while the discharge time is quite stable. The result is a decreasing pulse width for the charge and a relatively constant pulse width for the discharge of the internal capacitance. The reverse situation occurs for $\Delta Vt < -2.5V$. The reason is still unknown. Another difficulty arises because the ATD response combines with the output buffer characteristic.

If dynamic circuits prove to be efficient after irradiation, the correct design of an ATD will be required.

Other architecture's are possible for this address transition detection circuit. Here again, we have to avoid NOR and OR gates to achieve a good radiation hardness.

3.2.10. Cell scalability

In summary we may recall the favorable tendencies
for the static write operation:

- size increase of the write circuit inverter
- size increase of the write circuit pass gate
- size increase of the cell pass gate
- size decrease of the static bit line load
- size decrease of the pull-up transistor of the cell.

for the static read operation:

- size decrease of the cell pass gate.
- size increase of the pull-up transistor of the cell.

We assume that the whole circuit is correctly dimensioned such that the read and write operations are feasible before irradiation.
With n-channel pass transistors, the critical parameter is the read operation stability which seriously decreases due to the fall of n-channel resistivity.
With p-channel pass transistors, the critical parameter is the write operation ability which decreases due to the rise of p-channel resistivity.

The cell stability may be summarized by means of different curves:

- write operation with $wl_{push,cell}$ and $wl_{pass,cell}$ as variables, and with the threshold voltage as parameter.

In general, the static load do not affect strongly the write operation. The write operation is always easier for a small $wl_{push,cell}$ because less current is required to flip the cell internal state. With n-channel (p-channel) pass transistors, the write operation is easier (more difficult) after irradiation (Figs. 14 and 15).

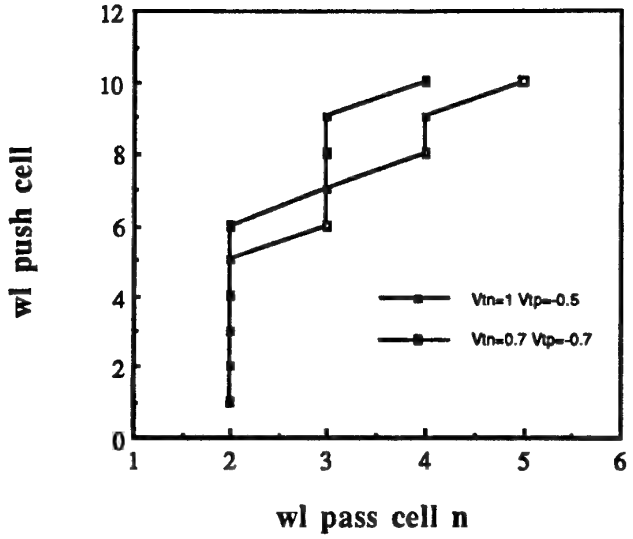


Figure 14: Write operation limit capability for n-channel pass transistors.

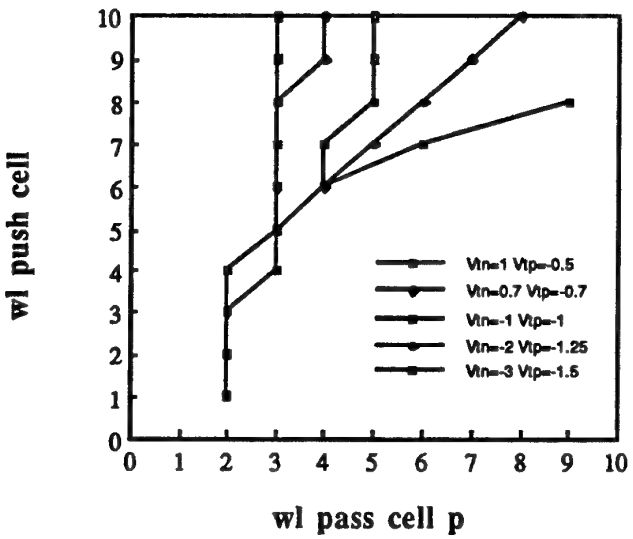


Figure 15: write operation limit for p-channel pass transistors.

- read or write operation with $V_{t,n}$ and $V_{t,p}$ as variables, and with $wl_{push,cell}$ as parameter. The read operation is critical for n-channel cell pass transistors (Fig.16) while the write operation is critical for p-type cell pass gate (Fig. 17).

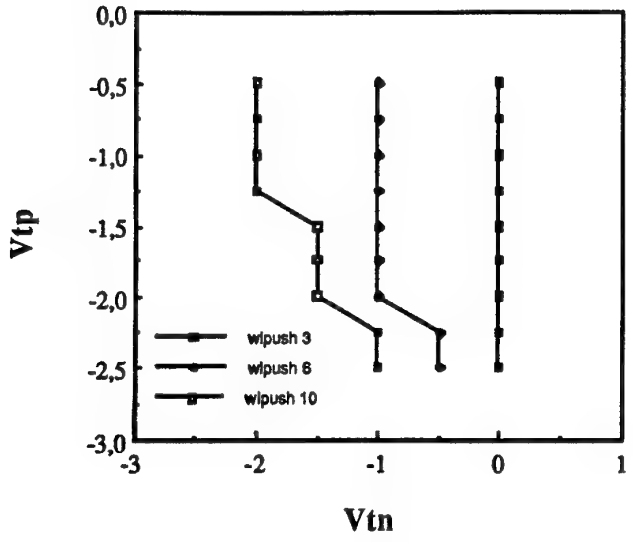


Figure 16: Read operation limit for n-channel pass transistors.

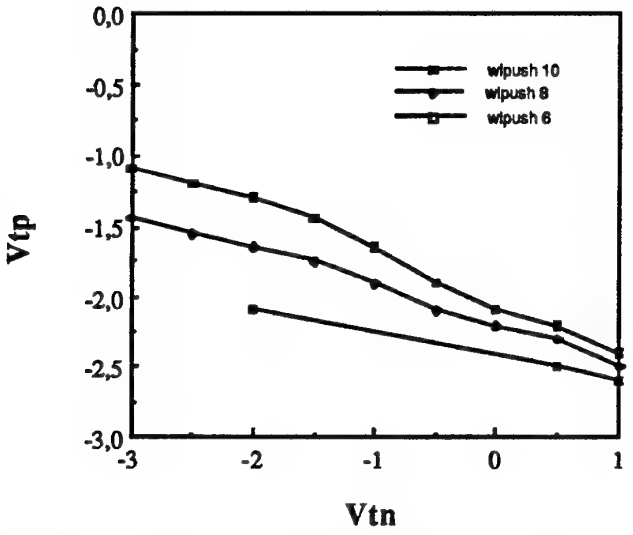


Figure 17: Write operation limit for p-channel pass transistors.

- inherent cell stability by means of the current or the voltage difference on the bit lines needed to flip the cell.

3.2.11. Implementation

We have implemented on the chip two 64-bit SRAM: one based on n-channel pass transistors (1) and the other on p-channel access gates (2). Separated write circuits (3,4,5) (with n-channel, p-channel pass transistor or three-state pass gate), read circuit (7) and basic decoder blocks (6) are available. An NAND gate (8), an inverter (9) and simple transistors (10,11) (n- and p-channel) will be useful in order to analyze total dose radiation effects. A schematic overview of the block disposition is shown in figure 18.

In order to find out the best memory cell design, every single of the 64 bits of the SRAMS has a design different from the other bits (different W/L ratios). This may yield non-functional bits on every memory chip, but will also indicate the best design which has to be repeated to obtain the best possible GAA SRAMs.

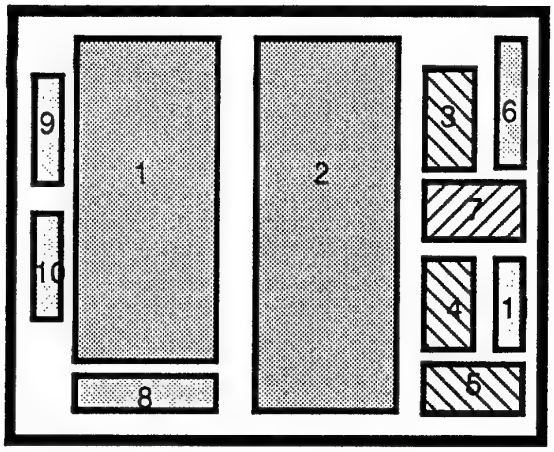


Figure 18: SRAM implementation,mask set MPCJAN93 (see text above for legend).

3.3. Hardness improvement through design

3.3.1. Introduction - Inverters

Total-dose hardening is usually achieved though he hardening of the individual transistors, at the process level or at the transistor design level. The aim of this Section is to develop design considerations which would help to render digital circuits almost insensitive to dose irradiation. The greatest problem that arises due to the threshold voltage negative shift are leakage currents in n-channel devices operating in the depletion mode.

Fig. 1 shows the simulated transfer characteristic of an inverter exposed to dose irradiation . Upon irradiation the switching point is shifted to the left because of threshold voltage shift but the most critical degradation is the high output level decrease due to a strong parasitic current flowing from the 'on' p-channel transistor to the ground through the 'off' n-channel device.

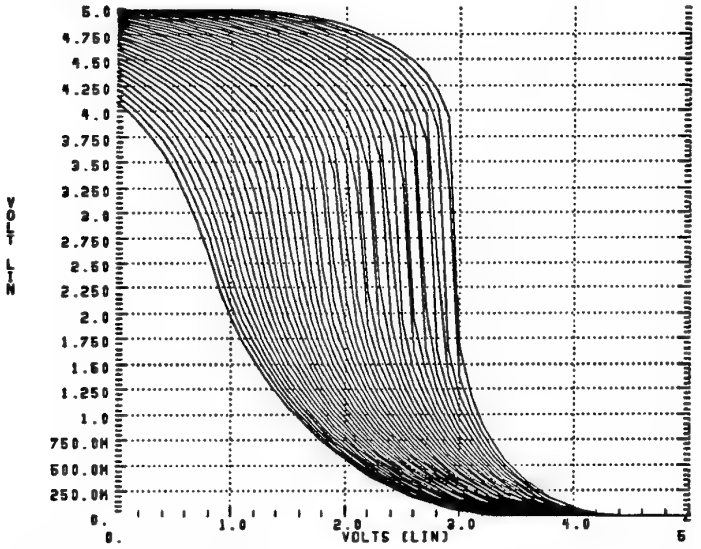


Figure 1: Transfer characteristic of a simple inverter. V_{tn} ranges from +1 to -3 V per 100 mV steps and V_{tp} ranges from -0.5 to -1.5 V per 25 mV steps, from right to left.

The only possibility to keep n-channel transistors off is to rise their source potential voltage to a sufficiently high value. Two basic designs may be investigated: either the combination of a pull-up p-channel transistor (AddTP) and a n-channel transistor (AddTN) introduced below the source of transistor N1 to be turned off (Fig. 2a), or simple transistors in the diode configuration inserted between the main inverter and the supply lines (Fig. 2b).

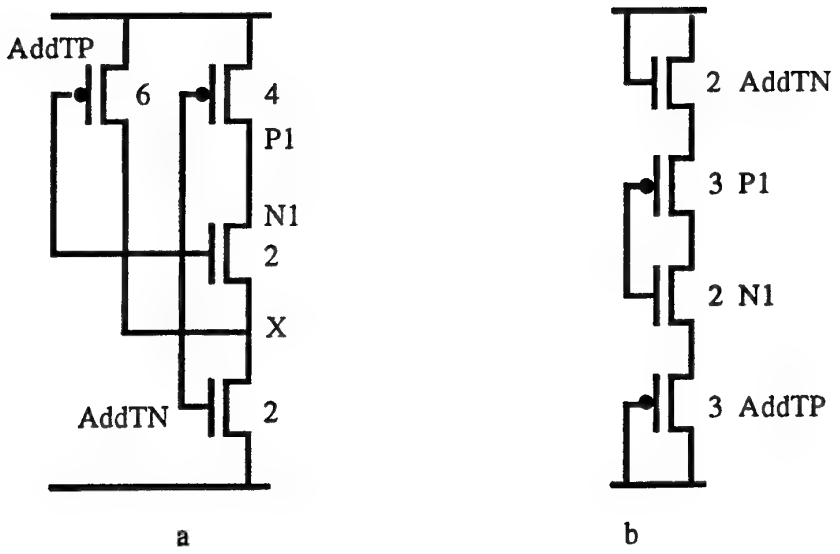


Figure 2: Improved inverters. a) with a pull-up configuration; b) with a diode pair.

In the first configuration (Fig. 2a), when the input bias is high, the additional p-channel transistor AddTP is off, AddTN is on and the initial circuit operation is not affected. AddTN and N1 are now in series. The new circuit is therefore slower but this may be overcome by doubling the size of each n-channel transistor. On the other hand, when the input voltage is low, the additional p-channel transistor pulls up the intermediate node X at a high level and therefore, N1 is more efficiently turned off. The transfer characteristic obtained with this circuit shows essentially an improvement of the high logic level now very close to V_{dd} (Fig. 3). As a consequence, the switching point shift is also slightly reduced. The (W/L) ratio of AddTP must be at least three times greater than the (W/L) ratio of AddTN to reach a significant improvement. The greater AddTP, the better the performances. This design is therefore very area-consuming especially if no speed performance reduction is allowed.

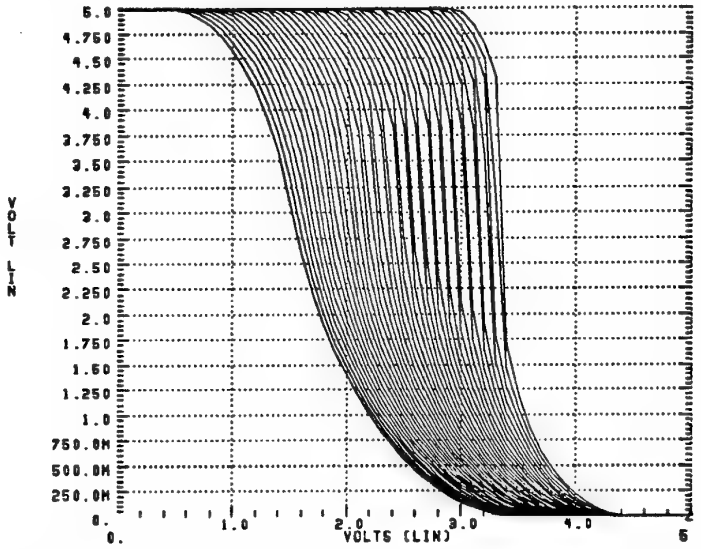


Figure 3: Transfer characteristic of the modified inverter shown at Fig. 2a. V_{tn} ranges from +1 to -3 V per 100 mV steps and V_{tp} ranges from -0.5 to -1.5 V per 25 mV steps, from right to left.

Another possibility is to enclose the initial inverter between a p-channel and a n-channel transistor in the diode configuration (Fig. 2b). The transfer characteristic of this inverter shows that the high logic level is V_{dd}-$V_{t,n}$, while the low output level is not zero but $V_{t,p}$ (these discrepancies unfortunately increase with total dose). The response of a chain of these inverters (to realize a buffer for example) produces neither a good high level nor a correct low output voltage. The advantage is that the shift of the switching point is drastically reduced (Fig. 4).

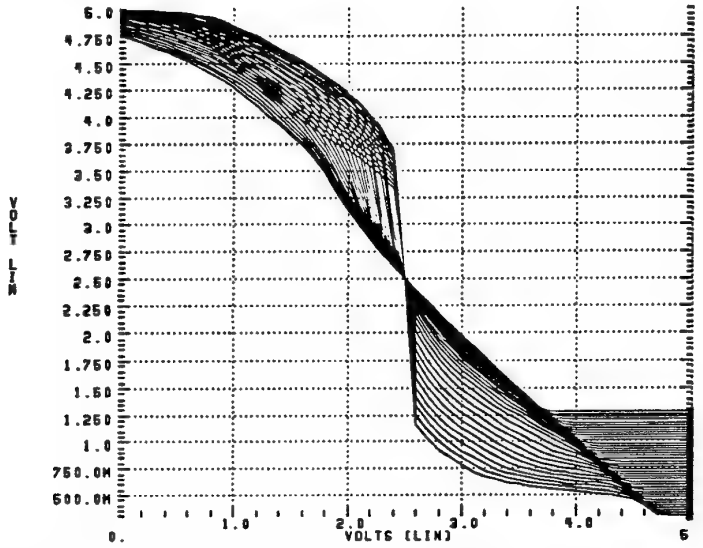


Figure 4: Transfer characteristic of the inverter depicted at Fig. 2b. V_{tn} ranges from +1 to -3 V per 100 mV steps and V_{tp} ranges from -0.5 to -1.5 V per 25 mV steps, from right to left.

An even less affected transfer characteristic (Fig. 5) is obtained by using a three-stage buffer combining the two improvements: the diode pair is introduced in the first stage to reduce the left shift of the transfer characteristic while the pull-up configuration is used in the following stages to maintain correct high and low output levels (Fig. 6).

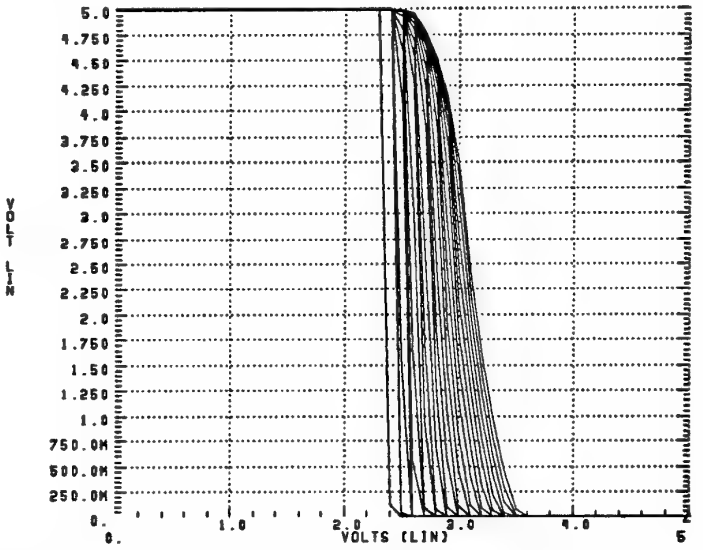


Figure 5: Transfer characteristic of the modified buffer shown at Fig. 6. V_{tn} ranges from +1 to -3 V per 100 mV steps and V_{tp} ranges from -0.5 to -1.5 V per 25 mV steps, from right to left.

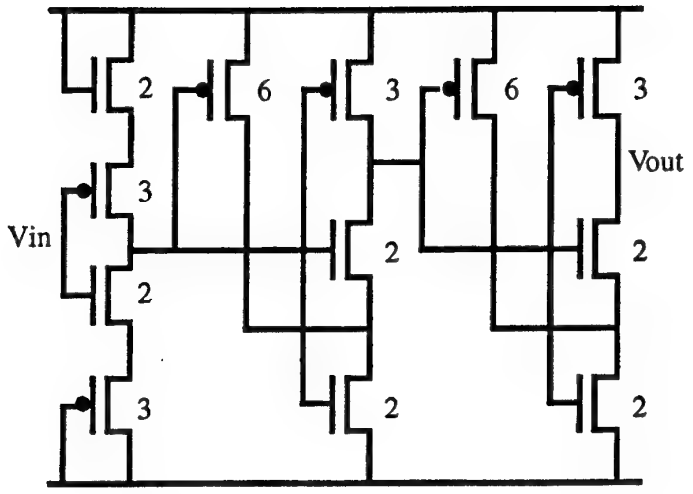


Figure 6: Three-stage modified buffer.

3.3.2. Pass gates

We have made several attempts to introduce similar improvements in pass gates (used to isolate write circuits and memory cells from bit and $\overline{bit}$ lines). No concluding results have emerged for nMOS pass transistors. In order to prevent a current flow through this pass gate in the isolation mode, the input node voltage must follow the output node voltage without modifying it. This is obviously impossible to implement since the output voltage is not fixed (as in an inverter) but may adopt any value between ground an supply voltage. The tri-state configuration is not able to provide a correct isolation due to the presence of a n pass transistor, either. Only the p pass transistor is adequate with the drawback of becoming more and more resistive when the total dose increases. Therefore, we must use p-channel transistors in all pass-gates, in the write circuits as well as in the cells. The circuit must be designed in order to allow a correct write operation after irradiation ((W/L) ratio of pass-transistors high enough), while simultaneously ensure a correct read operation before irradiation (with too high (W/L) ratio of pass transistors the read operation risks to flip the internal cell state).

3.3.3. Decoders

One may think that the improvement described for the inverter has to be implemented everywhere in the SRAM, but sometimes this it is not necessary. The full CMOS decoders, for example, are inherently sufficiently resistant. Only their last output inverter may be provided with the pull-up configuration in order to improve the high output voltage necessary to turn the p-channel pass-transistors off. This is not critical as if the high output level of the decoders decreases, $V_{t,p}$ of the controlled pass transistors decreases also. We did not have enough area on our chips to introduce such improvements.

3.3.4. Memory cells

The pull-up configuration may also be usefully introduced in each cell so that their high internal state could stay close to V_{dd}. This would improve the differential voltage appearing on bit and $\overline{bit}$ lines during the read operation. But this involves a great expense in the circuit area (which is more than doubled) and an over-dimensioning of the write circuits due to the non-negligible increase of the current necessary to flip the cell (+

25%). Therefore we chose to use normal cells (eventually with a slightly higher number of p-channel transistors in the cross-coupled inverters to improve the high internal state) and we carry back all the improvements on the differential sense amplifier. This read circuit has to be still very efficient after irradiation in order to amplify the decreasing differential voltage present on the bit lines.

3.3.5. Differential sense amplifier

Simulations show that better performance is obtained with a high (W/L) ratio for the source transistor, a small (W/L) ratio for the differential input pair and a high (W/L) ratio for the pull-up mirror devices.

Let us first examine the situation where Vin1 is low (left) and Vin2 is high (right). (Fig. 7a). The output voltage is nearly zero independently of the chosen (W/L) ratios. Indeed, the leakage current of the left n-channel transistor which is also flowing through the right n-channel 'on' transistor (due to the current mirror) fixes the output level. The output level could only depend on a difference between the $(W/L)_n$ ratios of the two input transistors. Assuming that they are equal, the output voltage is not influenced by the rest of the design. It is also clearly visible that the higher the source (W/L) ratio, the lower the output voltage.

The reverse situation (where Vin1 is high and Vin2 is low) is much more critical (Fig. 7b). In the ideal operation, a current flows in the left branch of the circuit and fixes the gate voltage of the right p-channel mirror transistor. This device must be considered as 'on'. If the right n-channel transistor is correctly turned off, the output voltage is high. If a leakage current is generated by this n-channel right transistor, it must also flow through the right p-channel mirror device and the output voltage decreases. The decrease is a function of $((W/L)_n:(W/L)_p)$. The resulting output voltage is closer to V_{dd} if $(W/L)_p$ is increased comparing to $(W/L)_n$.

With $(W/L)_p=15$, $(W/L)_n=1$ and $(W/L)_{source}=10$ and with a threshold voltage shift $DV_{t,n}=4*DV_{t,p}= -4V$, the output is 1V when $V_{in1}=0V$ & $V_{in2}=5V$ and is 4.65V when $V_{in2}=0V$ & $V_{in1}=5V$ (Fig. 8).

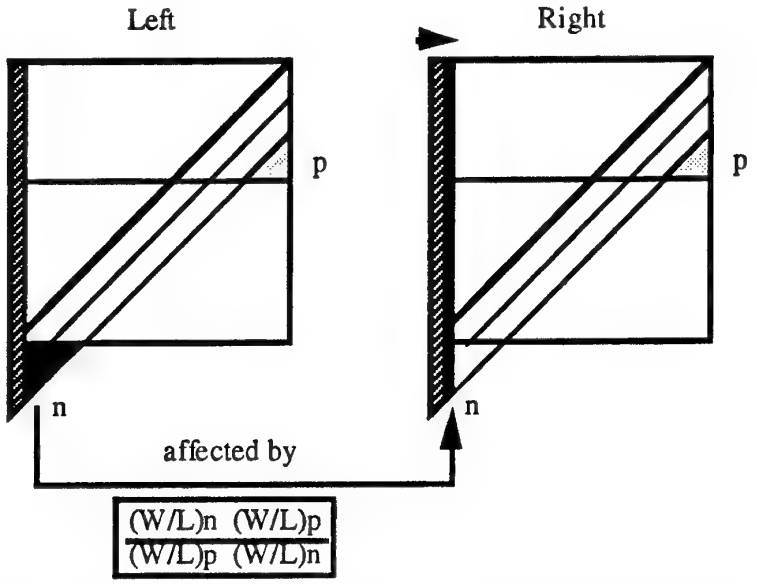


Figure 7a: Memelinck current diagram for the low output level.

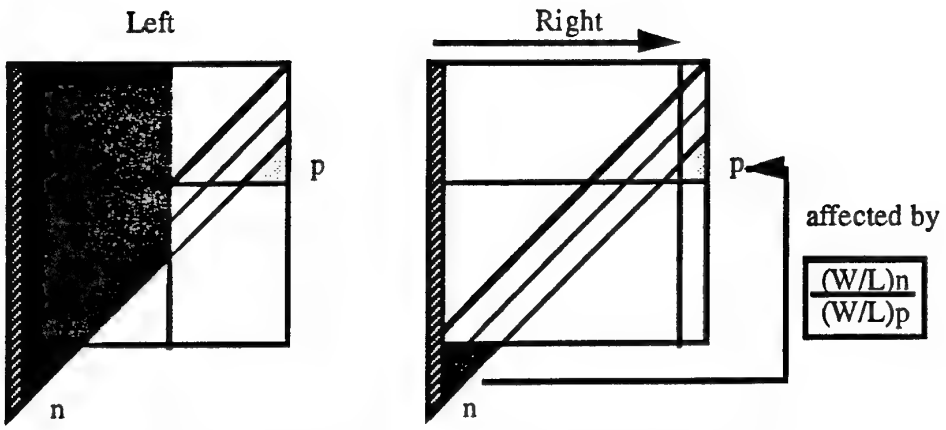


Figure 7b: Current diagram for the high output level.

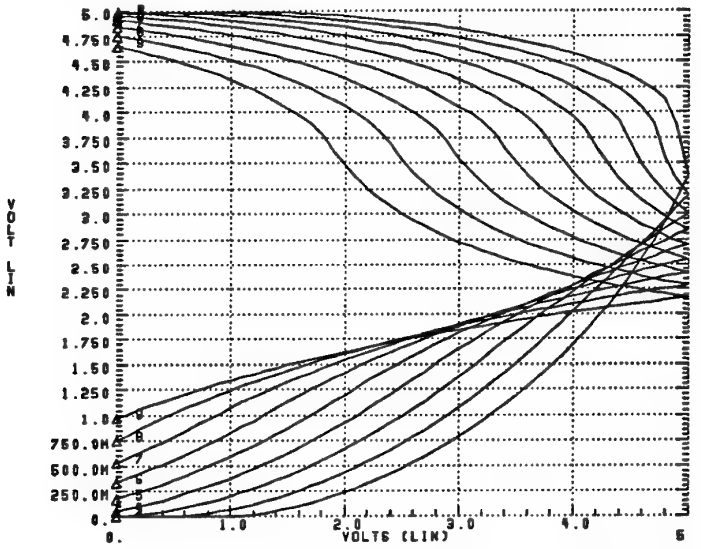


Figure 8: Characteristic of the read circuit while one input is kept at 5V and the other is swept form 0V to 5V.

As far as the source (W/L) ratio is concerned, we must also recall that all the read circuits work in parallel and feed the same output buffer. The output decoding operation relies on the isolation provided by these read circuits when their source transistor is off. Increasing the dose reduces this isolation and all the read circuits begin to influence each other. For this particular reason, it is preferable to limit the source (W/L) ratio.

Those results are not sufficient in comparison with the degradation of the high and low voltages imprinted by the cell on the bit lines during the read operation. We propose to introduce a pull-up configuration in both sides of the sense amplifier (Fig. 9). With the indicated (W/L) ratios and a threshold voltage shift $DV_{t,n}=4*DV_{t,p}=-4V$, the output is 0V as soon as Vin1<1.2 &Vin2=5V and is 5V as soon as Vin2<1.1 & Vin1=5V (Fig. 10). The sense amplifier response is now strongly and sufficiently improved to overcome the degradation introduced by the cells.

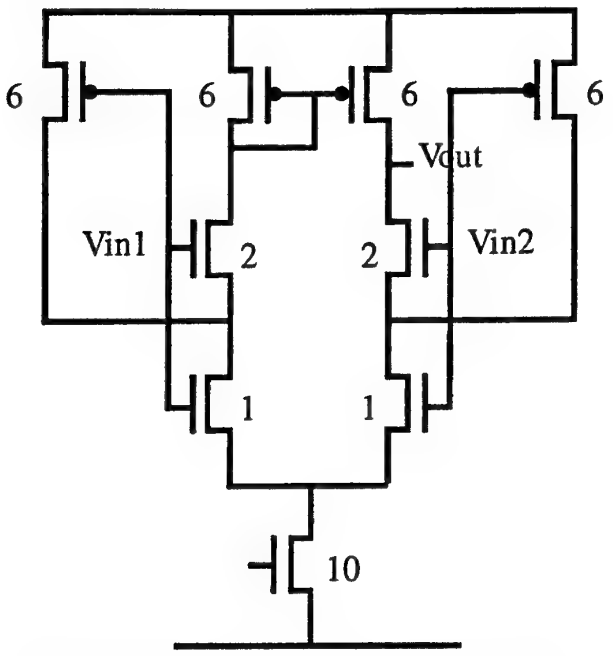


Figure 9: Modified differential sense amplifier.

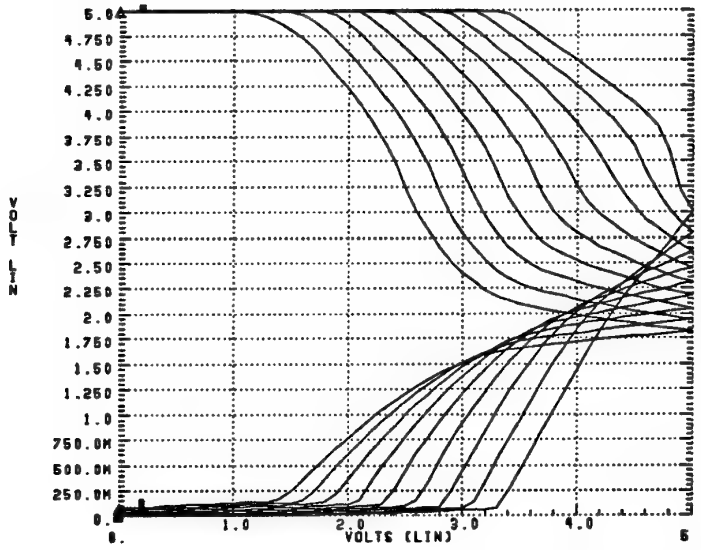


Figure 10: Characteristic of the modified read circuit while one input is kept at 5V and the other is swept form 0V to 5V.

We have previously determined that probably the best design of the read circuit consists in obtaining an output voltage equal to the switching point of the following buffer when 5V is applied at both inputs. Due to the increased p-channel mirror resistivity and the increased n-channel input pair driving ability, this output voltage (initially equal to about 2.5V) decreases under irradiation. The switching point of the output buffer also decreases due to total-dose effect. The global characteristic of these two circuits, considered as a whole, is therefore stable if the output decrease of the sense amplifier follows the shift of the buffer switching point. Therefore, we will not use our best improved buffer whose shift is negligible (and too small for the read circuit), but a buffer formed by three stages improved by the pull-up configuration. Adjusting the $(W/L)_p$ ratio in the read circuit and

the $(W/L)_p$ ratio in the buffer to obtain a similar decrease of V_{out} when $V_{in1}=V_{in2}=5V$ and the switching point we reach the results shown at figure 11.

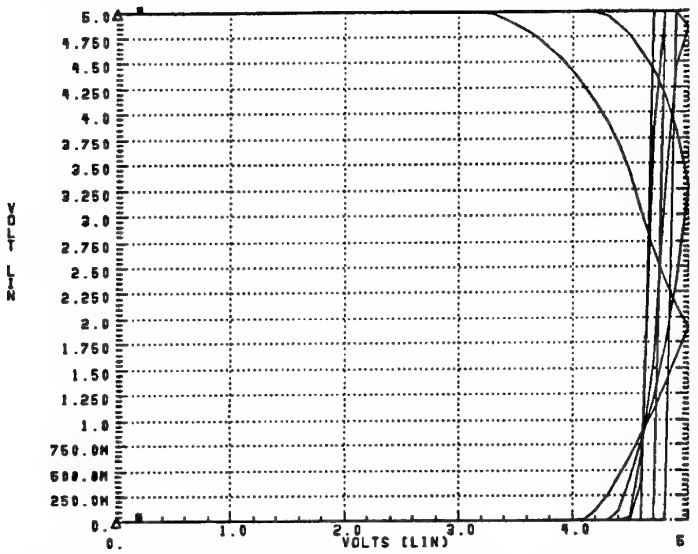


Figure 11: Characteristic of the modified read circuit followed by a modified buffer while one input is kept at 5V and the other is swept form 0V to 5V.

We have still to keep in mind that the sense amplifiers are connected in a parallel configuration and share the same output buffer. They have to select the correct output signal among the eight signals available on the different bit and $\overline{bit}$ lines. This function is ensured by the clock or source transistor of each read circuit which turns off such that the output of the inactive read cells do not degrade the selected output signal. As the radiation dose increases, it is more and more difficult to turn these clock transistors off and finally, the output signal becomes the mean value of all the outputs. Therefore, it is imperative to introduce one more additional pull-up transistor pair to rise the source of the clock device when it has to be turned off. Considering the available area on the chip, we have adopted the following design (Fig. 12):

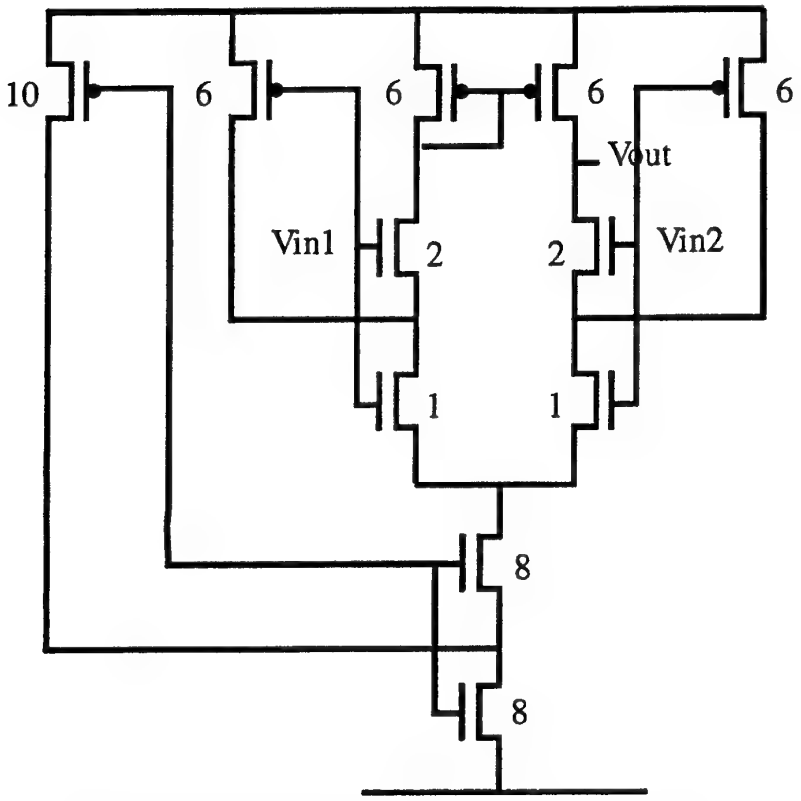


Figure 12: Final design of the differential sense amplifier.

We finally also introduce the pull-up configuration in write inverters. With all these improvements, we expect that the global memory will be fully efficient in the whole range of threshold voltage shift (ΔV_t going from 0V to -4V;$V_{t,n}$=-1V+ΔV_t; $V_{t,p}$=-0.5V+ΔV_t/4). All peripheral circuits filling a fixed and marginal circuit area were improved while the cells requiring most of the circuit space where kept as simple and smaller as possible.

3.3.6. Global compensation

3.3.6.1. Compensation for each n-channel device

We know that each transistor n of a given circuit may become radiation hard by adding a source pull-up pair in order to turn it off when necessary. This solution is not ideal for several reasons: first, 1 transistor n and 3 transistors p must be added for each transistor n. In order to keep the same speed performance, the size of the n-transistor and its pull-up pair must be doubled. The consumption of the global circuit is not reduced, as the initial leakage current of the n transistor is simply replaced by the current flowing through its corresponding pull-up pair. Finally, this design in case of NOR gates damage the output low level.

Let us imagine, Vin1=0 and Vin2=1. Vout must be 0V. The pull-up pair 1 increases Vs1 so that T1 turns off. The problem arises if T1 is not sufficiently turned off. In this case, Vout tends to follow Vs1 and the low output voltage degrades. This situation is more critical when more n transistors in parallel have to be turned off while the output voltage remains low. (Fig. 13a)

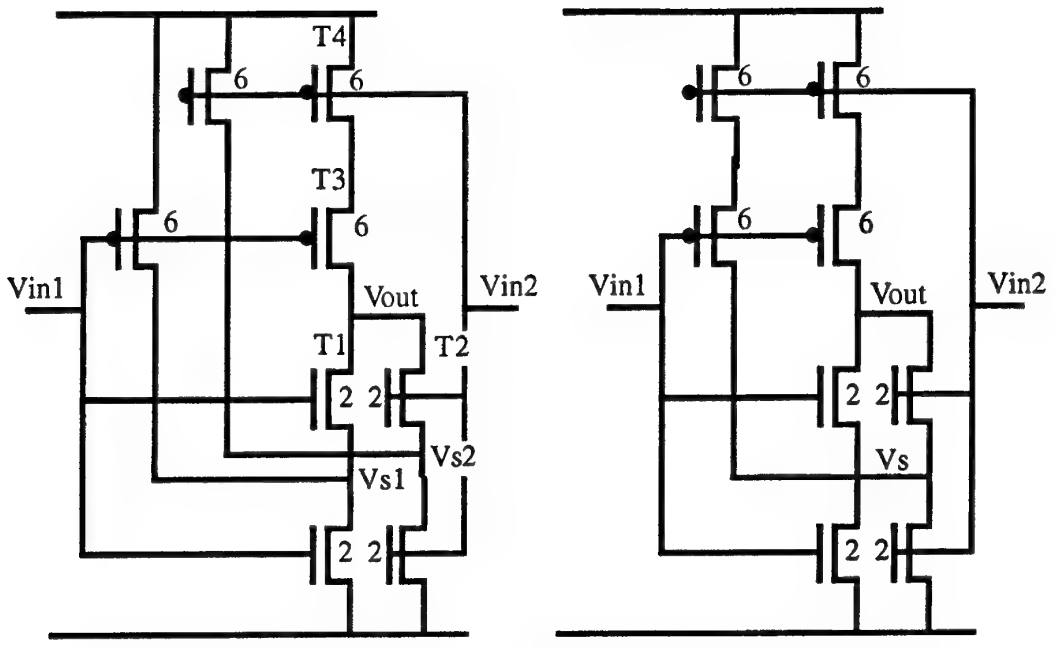


Figure 13: a) Pull-up pair for each transistor n of a NOR2 gate; b) Cascade of two NOR gates for $V_{t,n}$ compensation

To overcome this last problem, we may remark that a pull-up pair consists in fact of an inverter that rises the source voltage of the main inverter when necessary. Rather than compensating the $V_{t,n}$ shift transistor by transistor, we consider the gates as a whole. In this case, we use a NOR gate to rise the source voltage of the main NOR gate; a NAND gate to compensate the $V_{t,n}$ shift of the main NAND gate , etc... (Fig. 13b). In case of NAND gates, the design is exactly the same; in case of NOR gates, it brings some improvement.
With this compensation technique, we clearly see that the complexity of the circuit is doubled, the circuit area is usually more than doubled, and the global consumption is not reduced. Indeed, if the slave gate intends to turn the main gate off and therefore to annul the consumption, it unfortunately adds its own consumption similar to this of the main gate.

3.3.6.2. Global compensation

The next idea that emerges is to investigate a global compensation by means of only one pull-up pair or a single p-channel transistor. In this case, we will see that the complexity of the circuit, its area and its consumption may be reduced. The drawback is that we have to find somewhere the adequate signal to clock this compensation pull-up pair or transistor while slave NOR or NAND gates are simply fed with the usual inputs (Vin1, Vin2,...).

Three different circuits are proposed:

1 - A pull-up pair with the output signal of the main gate (NOR3) transformed by an inverter, as gate voltage (Fig. 14). The problem is that when the main gate is off, the input signals are no longer able to turn the gate on again, as far as $V_{t,n}>0$. The feedback loop is unfortunately locked. As far as Vt,n>0, Vs=5V when $\overline{Vout}$ =0V

and therefore, V_{out} stays at 5V even if the input signals turn the n-transistors of the main gate on again.

This problem disappears if we supply the pull-up pair with Vref=3V or less. With such an external bias, the global retroaction is weakened so that the main gate could be turned on again even if $V_{t,n}>0$, but the efficiency of the source voltage rising effect is also reduced. This system can afford the compensation as long as $V_{t,n}>=-2V$. After that, the low output level $\overline{Vout}$ becomes to increase although the high output level $\overline{Vout}$ is preserved.

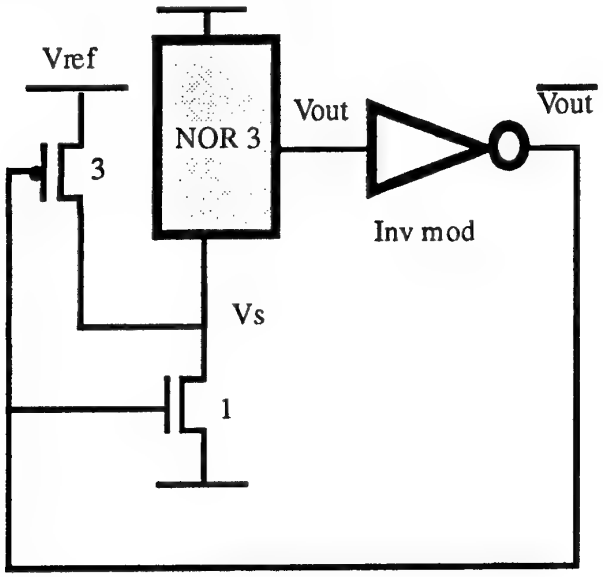


Figure 14: Static feedback by pull-up pair.

2 - The same circuit may be implemented with a normal supply equal to 5V at the condition that we add a reset transistor (Fig. 15). Before each evaluation of the output voltage, the reset transistor is activated which cuts the source voltage rising effect. The NOR3 gate is then able to evaluate its inputs. Once the clock transistor is off, the source voltage rising effect starts again if necessary. This method doesn't require an external intermediate bias Vref, but necessitates a dynamic clocking signal . Moreover, the output signal is only available at some precise moments. This system basically reaches the same results as the previous one.

Below $V_{t,n}=-2V$, both the low and high output voltages $\overline{Vout}$ fail.

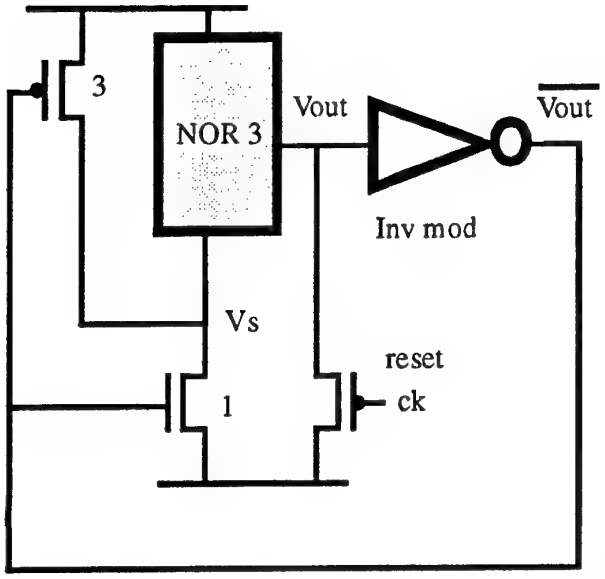


Figure 15: Dynamic feedback with pull-up pair and reset transistor.

3 - with the same dynamic reset process, a single p-transistor may replace the pull-up pair (Fig. 16). The gate voltage of the source rising transistor is here V_{out} rather than the output of the inverter. Good performances are obtained especially as far as the consumption is concerned because the p-channel transistor provides a perfect isolation when it is off. The drawback is that the low level of the output Vout cannot decrease below abs(Vt,p) and unfortunately degrades with the irradiation.

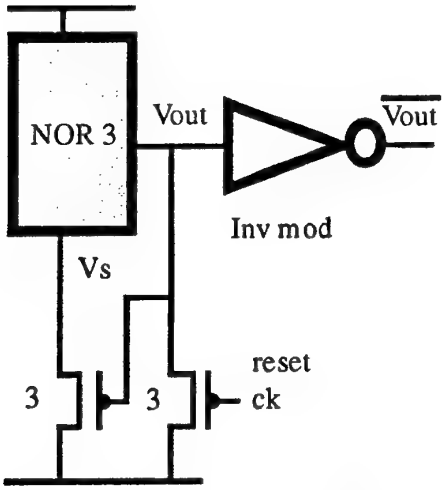


Figure 16: Dynamic feedback with p-channel transistor and reset device.

Vt,n (V)	A	B	C	D	E
Vin1=0V	Vin2=0V	Vin3=0V	Vout		
1	5	5	5	5	5
0,5	5	5	5	5	5
0	5	5	5	5	5
-0,5	4.6	5	5	5	5
- 1	3.9	5	5	5	5
-1,5	1.9	5	5	5	5
- 2	0.8	5	5	5	5
-2,5	0.6	5	4.55	5	5
- 3	0.5	5	1.3	1.4	5
Vin1=0V	Vin2=0V	Vin3=0V	Vout,bar		
1	0	0	0	0	0
0,5	0	0	0	0	0
0	0	0	0	0	0
-0,5	0	0	0	0	0
- 1	0	0	0	0	0
-1,5	4.3	0	0	0	0
- 2	4.75	0	0	0	0
-2,5	4.7	0	4	0	0
- 3	4.6	0	4.4	4	0
Vin1=0V	Vin2=0V	Vin3=1V	Vout		
1	0	0	0	0	0.7
0,5	0	0	0	0	0.8
0	0	0	0	0	0.85
-0,5	0	0.15	0	0	1.0
- 1	0	0.35	0	0	1.1
-1,5	0	0.55	0	0	1.2
- 2	0	0.8	0	0	1.3
-2,5	0	1.05	0	4.5	1.4
- 3	0	1.35	0	0	1.5
Vin1=0V	Vin2=0V	Vin3=1V	Vout,bar		
1	5	5	5	5	5
0,5	5...4.75	5	5	5	5
0	5...4.75	5	5	5	5
-0,5	5...4.75	5	5	5	4.95
- 1	5...4.75	5	5	5	4.85
-1,5	5...4.75	4.9	4.975	4.975	4.7
- 2	5...4.75	4.75	4.91	4.91	4.5
-2,5	5...4.75	4.5	4.85	0	4.2
- 3	4.75	4.35	4.75	4.75	3.6
Conclusion	valid	for	Δ Vt,n		
from ... to...	0V->2V	0V->4V	0V->3V	0V->3V	0V->4V

Table 1: NOR3 with different compensation techniques. Low and high level of the static transfer curve ($V_{t,n0}$=1V; $V_{t,p0}$=-0.5V; $\Delta V_{t,n}=4*\Delta V_{t,p}$).
a) Without compensation; b) Pull-up pair for each transistor n;
c) Feedback with pull-up pair and external Vref;
d) Feedback with pull-up pair and reset transistor;
e) Feedback with p-transistor and reset device.

Vt,n (V)	Inv	A	B	C	D ck=5V	D ck=0V	E ck=5V	E ck=0V
Vin1=0	Vin2=0	Vin3=0	Consum					
0	0	0	0	0	<4µ	400µ	<1µ	150µ
0.5	0	0	0	0	<4µ	410µ	<1µ	200µ
1	0	0	0	0	<4µ	450µ	<1µ	250µ
1.5	25µ	25µ	40µ	10µ	15µ	475µ	<1µ	325µ
2	75µ	100µ	100µ	30µ	40µ	525µ	<6µ	400µ
2.5	150µ	675µ	220µ	70µ	75µ	550µ	<6µ	410µ
3	250µ	620µ	350µ	110µ	120µ	675µ	<6µ	460µ
3.5	350µ	675µ	525µ	800µ	900µ	800µ	<6µ	500µ
4	475µ	760µ	700µ	850µ	850µ	850µ	<6µ	510µ
Vin1=0	Vin2=0	Vin3=1	Consum					
0	0	0	0	0	0	0	0	0
0.5	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	25µ	50µ
1.5	0	25µ	75µ	25µ	25µ	0	100µ	150µ
2	0	75µ	220µ	75µ	75µ	0	200µ	250µ
2.5	0	150µ	450µ	150µ	150µ	0	350µ	375µ
3	0	250µ	750µ	250µ	250µ	0	500µ	575µ
3.5	0	350µ	1050µ	350µ	350µ	0	600µ	600µ
4	0	475µ	1300µ	475µ	475µ	0	650µ	650µ
Conclusion								
consumpt. due to:	inv reset	NOR3 no leakage	3 pull-up reset	1 pull-up	1pull-			
	no leakage	out inv	>out inv	out inv	out inv	?	>>out inv	?

Table 2: NOR3 with different compensation techniques. Consumption.
($V_{t,n0}$=1V; $V_{t,p0}$=-0.5V; $\Delta V_{t,n}=4*\Delta V_{t,p}$).
a) Without compensation; b) Pull-up pair for each transistor n;
c) Feedback with pull-up pair and external Vref;
d) Feedback with pull-up pair and reset transistor;
e) Feedback with p-transistor and reset device.

Let us now draw some conclusions from Tables 1 and 2. The initial values of the threshold voltage are $V_{t,n}$=1V, $V_{t,p}$=-0.5V. We assume further that $\Delta V_{t,p}=\Delta V_{t,n}/4.0$.

As far as the static transfer curve is concerned:

- For the simple NOR3 gate: V_{out} high is degraded with increasing dose due to the leakage of n-type transistors. V_{out} low is of course perfectly maintained. Unacceptable high level is obtained for $V_{t,n}$<-1V.

- NOR3 gate with a pull-up pair for each transistor n: The high output level is correctly maintained due to the source voltage rising effect. But the low output level is slightly degraded due to the conflict between the source voltage rising effect and the low voltage that must be kept at the output.

- NOR3 gate embedded in a static feedback (pull-up pair supplied with Vref=3V): The high output voltage is perfect as far as the global feedback works ($\Delta V_{t,n}$>=-2V). The low output voltage is correct whatever the value of $\Delta V_{t,n}$.

- NOR3 gate embedded in a dynamic feedback N (pull-up pair supplied with 5V and p-channel reset transistor externally clocked): As far as the feedback is valid, the high output voltage is correctly maintained at 5V and the low output level is 0V. Beyond this point, the system fail.

- NOR3 gate embedded in a dynamic feedback P (p-channel device and p-channel reset transistor externally clocked): The high output level is always correct due to the perfect isolation of the p-type transistor but the low output level is degraded and cannot decrease below abs($V_{t,p}$).

As far as the consumption is concerned:

- For the improved inverter, if V_{in}=0V, the n-type transistor is not well turned off and a static current flows through the circuit. When V_{in}=5V, the p-type transistor is turned off and no leakage appears in the circuit.

- For the simple NOR3 gate, when Vout is high, the output inverter does not add any contribution to the leakage current. The leakage is only due to the 3 off n-channel transistors in the NOR3 gate. This leakage is appreciably higher than for an improved inverter. When Vout is low, the gate does not leak but the output inverter adds its contribution.

- NOR3 gate with a pull-up pair for each transistor n, when V_{out} is high, the leakage is due to all the pull-up pairs, working simultaneously. The global consumption is very similar to the initial consumption of the NOR3 gate without improvement. When Vout is low, the leakage is only due to the output inverter fed with an input voltage which stays not very close to 0V. Therefore, the consumption is higher than this mentioned for an inverter fed with an ideal input voltage of 0V.

- NOR3 gate embedded in a static feedback (pull-up pair supplied with Vref=3V): when Vout is high, the consumption is due to the pull-up pair. As long as the feedback works, the consumption is reduced by a factor of 3 compared to the simple NOR3 gate. If the consumption is reduced, the circuit speed is reduced too. Therefore, this improvement is not significative since it results from the under-dimensionning of the pull-up pair. When Vout is low, the consumption is only due to the output inverter.

- NOR3 gate embedded in a dynamic feedback N (pull-up pair supplied with 5V and reset p-channel transistor externally clocked): when CK=5V (reset transistor off): the consumption is due to the pull-up pair when Vout is high (reduction by a factor of 3; same remark as above) and to the output inverter when Vout is low. When CK=0V, the consumption dramatically increases due to the static path present between Vdd and Gnd. This consumption may be kept within reasonable limits by reducing the time allowed to the reset process.

- NOR3 gate embedded in a dynamic feedback P (p-channel device and p-channel reset transistor externally clocked). When CK=5V (reset transistor off), the consumption is nearly zero if Vout is high and is due to the output inverter fed with a bad output voltage if Vout is low (consumption therefore increased compared to an inverter ideally fed of 0V). With CK=0V, the static path between supply and ground gives rise to a non negligible consumption that could be limited in time.

The results are slightly different according to the design of the output inverter.

3.3.7. Implementation

Two chips were allowed to the GAA study in the mask set MPCMAY93.
The first one is identical to the chip designed in the mask set MPCJAN93 except that the inverter is replaced by a NAND2 and the NAND2 is replaced by the output buffer.

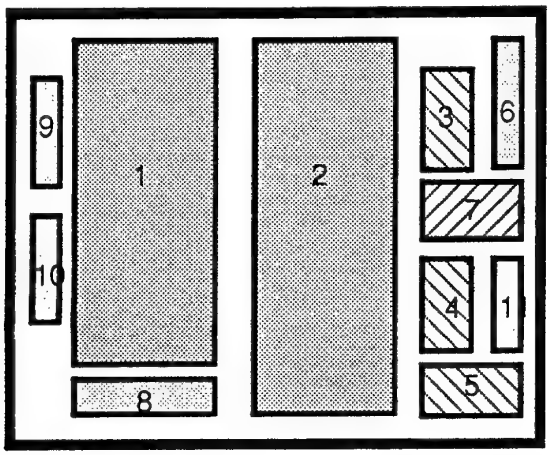


Figure 17: MPCMAY93-chip 1: 1. SRAM N ; 2. SRAM P; 3. WriteN ; 4. WriteP; 5. WriteTri; 6. Read; 7. Dec; 8. Buffer; 9. NAND2; 10. nMOSmin; 11. pMOSmin

The second chip (MPCMAY93) contains:

- an SRAM with
  - normal cells with p-channel pass transistors W/L=4 et W/L=8, number of p transistors/number of n transistors: 3...10
  - normal decoders
  - improved write cells (pull-up pair in the inverter and p-type pass transistor W/L=10)
  - improved read cells and output buffer
  - static or dynamic precharge
- the modified read circuit + the new output buffer: one pad is provided for the clock transistor
- the new output buffer alone
- the separated new write circuits: n and p pass transistors and tristate: two pads are provided for gate of the precharge transistors. If they are connected to Vdd or gnd, they simulate a dynamic charge, if they are externally connected to out1 and out2 respectively, they simulate a static charge. One pad is also used to clock the pass transistor or tristate configuration and check the isolation.
- two capacitance structures (GAA n and p transistors in parallel + the calibration structure)
- an operational amplifier
- five structures to check the effect of a global compensation of the Vt shift:
  - NOR3 without compensation
  - NOR3 with a pull-up pair for each n transistor
  - NOR3 with a single pull-up pair and a reference bias (Vref=3V)
  - NOR3 with a single pull-up pair and a reset transistor (CK)
  - NOR3 with a p-type transistor and a reset device (CK).

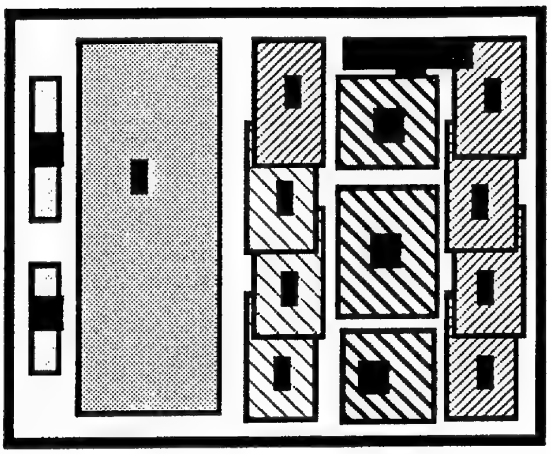
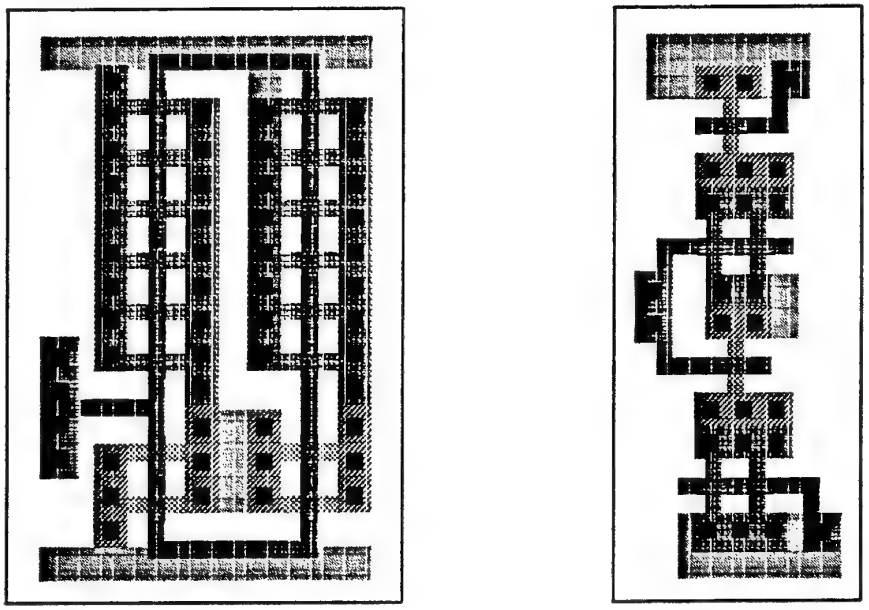


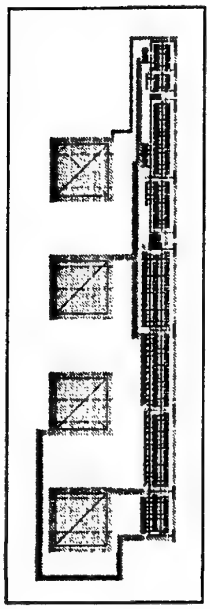
Figure 18: MPCMAY93-chip 2: 1. SRAM P; 2. WriteP; 3. WriteN; 4. WriteTri;
5. NOR3stat; 6. NOR3; 7. NOR3eachn; 8. NOR3dynPull; 9. NOR3dynP;
10. Read; 11. Buffer; 12. Inverter; 13. Capas; 14. Amplifier.

3.3.7.1. Layouts

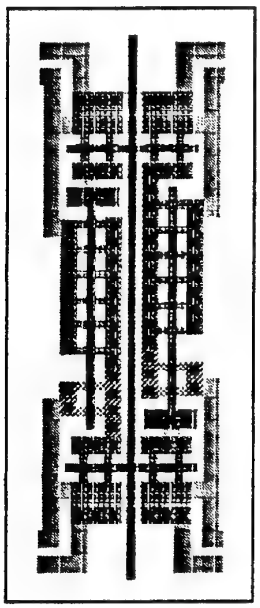


a b

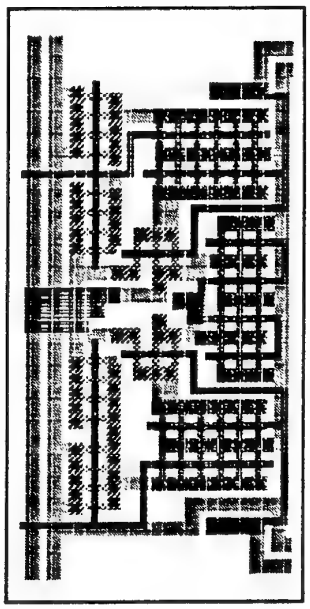
Layouts: a) Modified invertor with a pull-up configuration; b) Modified invertor with a diode configuration.



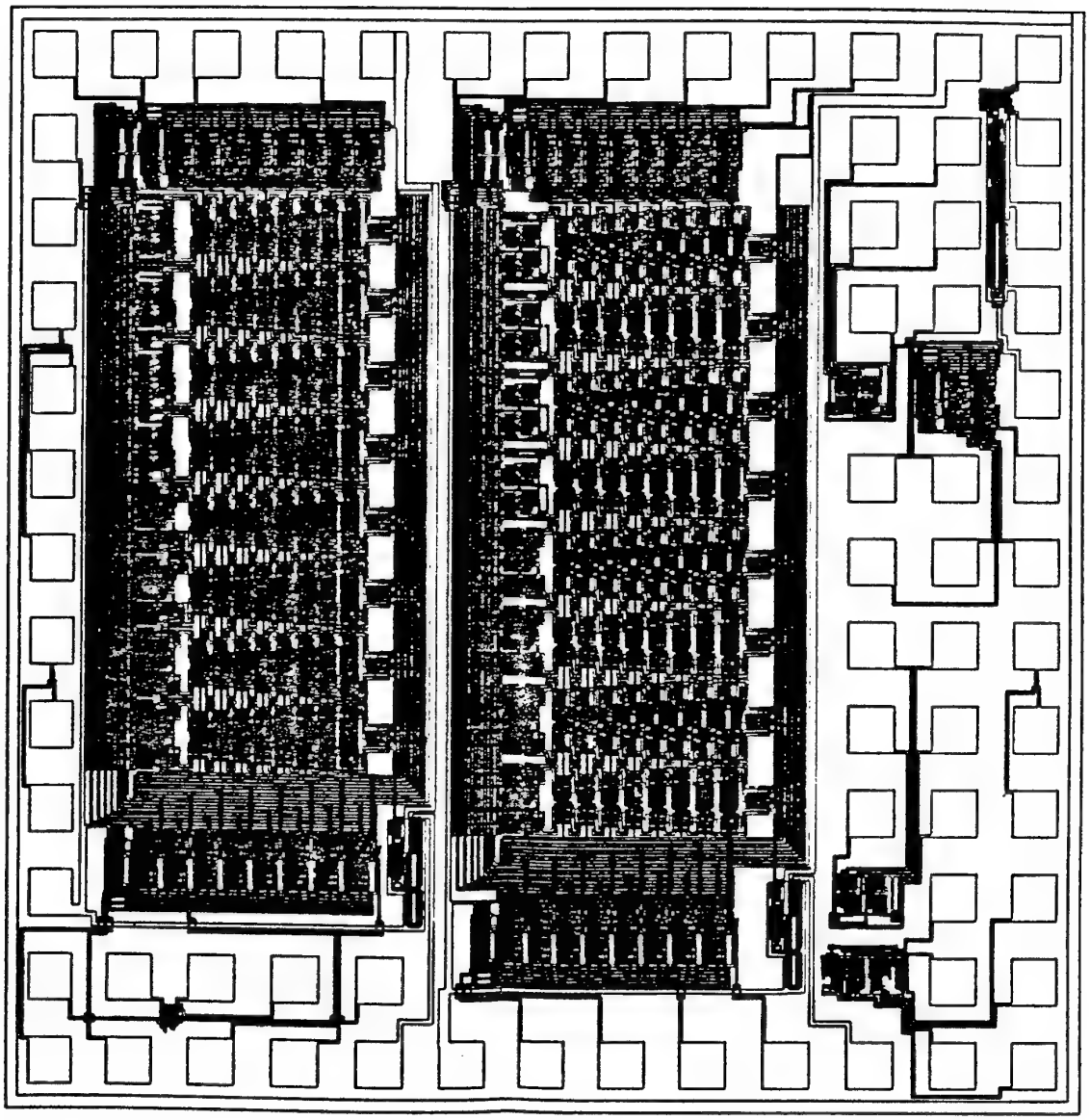
Layout of a modified buffer: three stages in the ratio 1:3:9 with the pull-up configuration.



Layout of a memory cell.



Layout of a differential sense amplifier.

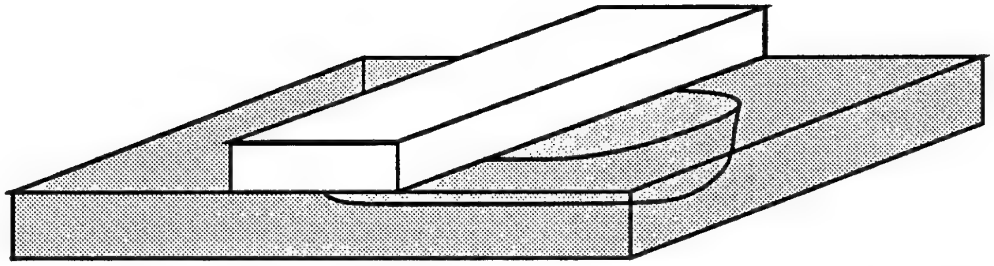


Layout of two 64k SRAMs.

4. Processing

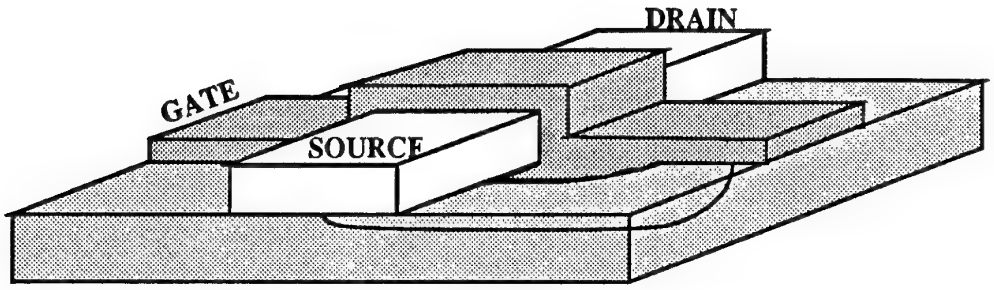
4.1. N-channel devices

The process starts with standard SIMOX wafers. The thickness of the starting silicon film is 200 nm . After film thinning down to a thickness of 125 nm, a 30 nm-thick pad oxide is grown, and a 200 nm-thick film of silicon nitride is deposited. A mask step is used to pattern the nitride as well as the silicon film in a dry etch reactor. Using the nitride as a mask, 250 nm of oxide are grown on the edge of the silicon island. Such an oxidation as for consequence to smooth the edges of the silicon island and has been reported to be useful to improve gate oxide breakdown properties. The nitride and the pad oxide are then wet etched, and a second masking step is used to define areas where the underlying oxide (as well as the edge oxide) will be etched. Etching of the buried silicon leaves a beam (bridge) of silicon free-standing over a cavity (Figure below) The silicon bridge is supported at both ends by the original buried oxide. The free-standing part of the silicon island will later on become the active part of the device (the channel region), while those parts still supported by the underlying oxide will become the source and the drain.



Gate-All-Around device after etching of a cavity underneath the silicon island

A thick thermal gate oxide is then grown at 850°C in dry oxygen. Its thickness is 30 nm. Boron is there implanted to adjust threshold voltage. A 400 nm-thick polysilicon film is the deposited in a LPCVD furnace at a temperature of 620°C. Because of the excellent conformal deposition of LPCVD polysilicon, gate material is deposited not only at the top of the device, but also in the cavity below the silicon bridge. Polysilicon is, hence, deposited all around the gate oxide which itself is grown all around the channel region of the silicon island (hence the name: Gate-All-Around Device.) The polysilicon film is then implanted with phosphorous ions, and a long (2 hours) annealing step is used to diffuse the phosphorous everywhere in the polysilicon, even underneath the silicon bridge, where no ions are implanted. The polysilicon is then etched using a mask step to define the gate, after which phosphorous is implanted to form self-aligned sources and drains (Figure below) After source and drain anneal, low temperature oxide is deposited, and contact hole are etched. A standard metallization step completes the process. Care is taken not to use steps at temperatures higher than 850°C after the gate oxide has been grown.



Gate-All-Around device after source and drain formation

4.2. P-channel devices

The process starts with standard SIMOX wafers. The thickness of the starting silicon film is 200 nm . After film thinning down to 125 nm, a 30 nm-thick pad oxide is grown, and a 200 nm-thick film of silicon nitride is deposited. A mask step is used to pattern the nitride as well as the silicon film in a dry etch reactor. Using the nitride as a mask, 250 nm of oxide are grown on the edge of the silicon island. Such an oxidation as for consequence to smooth the edges of the silicon island and has been reported to be useful to improve gate oxide breakdown properties. The nitride and the pad oxide are then wet etched, and a second masking step is used to define areas where the underlying oxide (as well as the edge oxide) will be etched. Etching of the buried silicon leaves a beam (bridge) of silicon free-standing over a cavity.The silicon bridge is supported at both ends by the original buried oxide. The free-standing part of the silicon island will later on become the active part of the device (the channel region), while those parts still supported by the underlying oxide will become the source and the drain. The gate oxide is then grown at 850°C in dry oxygen. Its thickness is 30 nm . Boron is there implanted to adjust threshold voltage. A 400 nm-thick polysilicon film is the deposited in a LPCVD furnace at a temperature of 620°C. Because of the excellent conformal deposition of LPCVD polysilicon, gate material is deposited not only at the top of the device, but also in the cavity below the silicon bridge. Polysilicon is, hence, deposited all around the gate oxide which itself is grown all around the channel region of the silicon island (hence the name: Gate-All-Around Device.) The polysilicon film is then implanted with phosphorous ions, and a long (2 hours) annealing step is used to diffuse the phosphorous everywhere in the polysilicon, even underneath the silicon bridge, where no ions are implanted. The polysilicon is then etched using a mask step to define the gate, after which phosphorous is implanted to form self-aligned sources and drains. After source and drain anneal, low temperature oxide is deposited, and contact hole are etched. A standard metallization step completes the process. Care is taken not to use steps at temperatures higher than 800°C after the gate oxide has been grown.

A lithography with minimum feature size of 3 μm was used for the process. Similar devices were made without etching a cavity underneath the silicon island. These devices are thus classical SOI MOSFETs, and can be used for comparing the electrical properties of Gate-All-Around devices and classical SOI MOSFETs, both before and after exposure to ionizing radiations.

4.3. Process modeling

The next pages present the SUPREM-IV simulation files used to model the Gate-All-Around fabrication process as well as the result of MEDICI simulations of the device behaviour.

```
$ TMA TSUPREM-4 GAA N-channel Structure
option device=X
$ Specify x mesh
LINE X LOCATION=0 SPACING=0.5 TAG=LEFT
LINE X LOCATION=1.5 SPACING=0.2
LINE X LOCATION=2.5 SPACING=0.2
LINE X LOCATION=3.5 SPACING=0.3 TAG=RIGHT

$ Specify y mesh
$LINE Y LOCATION=0  SPACING=0.02 TAG=OXTOP
LINE Y LOCATION=0.03 SPACING=0.015 TAG=OXBOTTOM
LINE Y LOCATION=2.0 SPACING=1.0 TAG=SIBOTTOM

$ELIMINATE COLUMNS X.MIN=1.8 X.MAX=5.2 Y.MIN=0.05
$ELIMINATE COLUMNS Y.MIN=0.03

$ Define isolation oxide and silicon substrate
$REGION  OXIDE XLO=LEFT XHI=RIGHT YLO=OXTOP  YHI=OXBOTTOM
REGION  SILICON XLO=LEFT XHI=RIGHT YLO=OXBOTTOM YHI=SIBOTTOM
INITIALIZE <100> arsenic=1E20
deposit oxide thickness=0.05 spaces=6

$ Deposit epi with nonuniform vertical grid spacing
DEPOSIT SILICON BORON=1E14 THICKNESS=0.1018 SPACES=10
$DEPOSIT SILICON BORON=1E17 THICKNESS=0.1 SPACES=5 DY=0.01

$ Plot initial mesh
SELECT  Z=1 TITLE="Initial Mesh"
PLOT.2D GRID Y.MAX=1 C.GRID=2
$PRINT.1D X.VALUE=0.0 LAYERS

$ Use vertical oxidation model to grow pad oxide
$METHOD  VERTICAL GRID.OXI=4
$DIFFUSE TIME=26 TEMP=1000 DRYO2

$SELECT  Z=1
$PRINT.1D X.VALUE=0.0 LAYERS
$etch oxide all
$select z=1
$print.1D x.value=1 layers

$gate oxide

method vertical grid.oxi=4
diffuse time=120 temp=950 dryo2
select z=1
print.1D x.value=1 layers
implant boron dose=3e12 energy=20
diffuse time=10 temp=950 dryo2
diffuse time=60 temp=800 inert

$ Deposit, dope, and pattern poly
DEPOSIT POLY THICK=0.5 SPACES=3
implant phosphorus dose=5e15 energy=100
```

```
DIFFUSE TIME=120 TEMP=800 inert
ETCH  POLY LEFT P1.X=2
etch oxide left P1.x=2
plot.2D boundary

$ Source/drain implant and anneal
IMPLANT ARSENIC DOSE=2E15 ENERGY=40
diffuse time=30 temp=800 dryO2
DIFFUSE TIME=180 TEMP=800
$ Metallization
DEPOSIT OXIDE THICK=0.4
ETCH  OXIDE LEFT P1.X=1.0 P2.X=1.1 P1.Y=-2 P2.Y=0.0
DEPOSIT ALUMINUM THICK=1
ETCH  ALUMINUM RIGHT P1.X=1.2 P2.X=1.3 P1.Y=-3 P2.Y=2

$ Reflect structure, then save complete MOSFET
STRUCTURE OUT.FILE=S4EX9S1
STRUCTURE REFLECT RIGHT
select z=1
plot.2d boundary x.min=0 x.max=7 y.min=-0.6 y.max=0.1

STRUCTURE OUT.FILE=gaanout PISCES

$ Plot grid & profiles for complete structure
SELECT  Z=DOPING TITLE="SOI MOSFET"
PLOT.2D Y.MAX=0.1 y.min=-0.2
$COLOR  SILICON COLOR=7
$COLOR  OXIDE  COLOR=5
$COLOR  POLY  COLOR=3
$COLOR  ALUMINUM COLOR=2
FOREACH X ( 16 TO 21 STEP 1 )
 CONTOUR VALUE=( 10^ X ) COLOR=4 LINE.TYP=2
 CONTOUR VALUE=(-(10^ X )) COLOR=2 LINE.TYP=5
END
PLOT.2D ^AX ^CL

PLOT.2D boundary SCALE Y.MAX=1 C.GRID=2

$ Plot 1D concentration profiles
SELECT  Z=LOG10(ACTIVE(BORON)) TITLE="Doping Profiles" +
  LABEL="log(Active Concentration)"
PLOT.1D X.VALUE=1 BOTTOM=15 TOP=21 LEFT=-0.1 RIGHT=0 LINE.TYP=5
$   COLOR=2
LABEL  LABEL="Boron (x=1)" X=-0.1 Y=17

SELECT  Z=LOG10(ACTIVE(ARSENIC))
PLOT.1D X.VALUE=0 ^AXES ^CLEAR LINE.TYP=2
$COLOR=3
LABEL  LABEL="Arsenic (x=0)" X=-0.1 Y=20.3

$ Plot 1D concentration profiles
SELECT  Z=LOG10(ACTIVE(BORON)) TITLE="Doping Profiles" +
  LABEL="log(Active Concentration)"
PLOT.1D y.VALUE=-0.01 BOTTOM=15 TOP=21 LEFT=0 RIGHT=6 LINE.TYP=5 +
  COLOR=2
LABEL  LABEL="Boron (x=1)" X=-0.1 Y=17

SELECT  Z=LOG10(ACTIVE(ARSENIC))
PLOT.1D X.VALUE=0 ^AXES ^CLEAR LINE.TYP=2 COLOR=3
LABEL  LABEL="Arsenic (x=0)" X=-0.1 Y=20.3
```

MEDICI file , n-channel GAA device

```
$option device=X
mesh infile=gaanout tsuprem4 elec.bot poly.ele
$ comment electrodes source=1 gate=3 drain=2 substrate=4
contact number=3 n.poly
interfac qf=2e11
plot.2d junction boundary y.max=0.1 y.min=-0.15 x.min=0 x.max=7
plot.1d doping x.start=0 x.end=7 top=1e20 bottom=1e14 y.start=-0.07
+ y.end=-0.07 Y.logari
$models conmob consrh bgn prpmob
$material silicon n.ioniza=1e6 ecn.ii=2.54e6 taup0=2e-8
symb carriers=0
solve v3=-0.5 v2=0.1 V4=-0.5 V1=0 init
$plot.2d boundary depletio y.max=0.01 y.min=-.15
$stop
symb carriers=1 electrons newton
method autonr
solve out.file=n2init
solve v2=0.1 v3=-0.5 v4=-0.5 pre
log ivfile=gaanvt
solve pro v1=0 v2=0.1 V4=-0.5 v3=-0.5 elec=(3,4) vstep=0.2 nstep=10


plot.1D x.axis=V3 y.axis=I2 left=-0.5 right=2 bot=0
plot.1d x.axis=V3 y.axis=I2 left=-0.5 right=2 y.logari bot=1e-14 top=1e-4
stop
$load in.file=n2init
models conmob consrh bgn prpmob impact.i
symb carriers=2 newton
$solve v1=0 v2=0 v3=0 v4=0 pre
$solve v1=0 v2=0 v3=1 v4=0 pre out.file=n2init
$log ivfile=n2vd1
$solve v1=0 v2=0 v3=1 v4=0 pro elec=2 vstep=0.2 nstep=25
$plot.1D x.axis=v2 y.axis=i2 left=0 right=5 bot=0

$load in.file=n2init
$solve v1=0 v2=0 v3=2 v4=0 pre out.file=n2init
$log ivfile=n2vd2
$solve v1=0 v2=0 v3=2 v4=0 pro elec=2 vstep=0.2 nstep=25
$plot.1d x.axis=v2 y.axis=i2 left=0 right=5 bot=0

$load in.file=n2init
$solve v1=0 v2=0 v3=3 v4=0 pre out.file=n2init
$log ivfile=n2vd3
$solve v1=0 v2=0 v3=3 v4=0 pro elec=2 vstep=0.2 nstep=25
$plot.1d x.axis=v2 y.axis=i2 left=0 right=5 bot=0

$load in.file=n2init
$solve v1=0 v2=0 v3=4 v4=0 pre out.file=n2init
$log ivfile=n2vd4
$solve v1=0 v2=0 v3=4 v4=0 pro elec=2 vstep=0.2 nstep=25
$plot.1d x.axis=v2 y.axis=i2 left=0 right=5 bot=0

$load in.file=n2init
$solve v1=0 v2=0 v3=5 v4=0 pre
$log ivfile=n2vd5
$solve v1=0 v2=0 v3=5 v4=0 pro elec=2 vstep=0.2 nstep=25
$plot.1d x.axis=v2 y.axis=i2 left=0 right=5 bot=0


solve v1=0 v2=0 v3=0 v4=0 pre
solve v1=0 v2=0 v3=0 v4=-1 pre
```

```
solve v1=0 v2=0 v3=0 v4=-2 pre
solve v1=0 v2=0 v3=0 v4=-3 pre
solve v1=0 v2=0 v3=0 v4=-4 pre
solve v1=0 v2=0 v3=0 v4=-5 pre out.file=n2init
solve v1=0 v2=0 v3=1 v4=-5 pre out.file=n2init
$log ivfile=n2vd1-5
$solve v1=0 v2=0 v3=1 v4=-5 pro elec=2 vstep=0.2 nstep=25
$plot.1d x.axis=v2 y.axis=i2 left=0 right=5 bot=0

$load in.file=n2init
solve v1=0 v2=0 v3=2 v4=-5 pre out.file=n2init
$log ivfile=n2vd2-5
$solve v1=0 v2=0 v3=2 v4=-5 pro elec=2 vstep=0.2 nstep=25
$plot.1d x.axis=v2 y.axis=i2 left=0 right=5 bot=0

$load in.file=n2init
solve v1=0 v2=0 v3=3 v4=-5 pre out.file=n2init
$log ivfile=n2vd3-5
$solve v1=0 v2=0 v3=3 v4=-5 pro elec=2 vstep=0.2 nstep=25
$plot.1d x.axis=v2 y.axis=i2 left=0 right=5 bot=0

load in.file=n2init
solve v1=0 v2=0 v3=3.5 v4=-5 pre out.file=n2init
solve v1=0 v2=0 v3=4 v4=-5 pre out.file=n2init
log ivfile=n2vd4-5
solve v1=0 v2=0 v3=4 v4=-5 pro elec=2 vstep=0.2 nstep=25
plot.1d x.axis=v2 y.axis=i2 left=0 right=5 bot=0

load in.file=n2init
solve v1=0 v2=0 v3=4.5 v4=-5 pre out.file=n2init
solve v1=0 v2=0 v3=5 v4=-5 pre out.file=n2init
log ivfile=n2vd5-5
solve v1=0 v2=0 v3=5 v4=-5 pro elec=2 vstep=0.2 nstep=25
plot.1d x.axis=v2 y.axis=i2 left=0 right=5 bot=0
```

```
$ TMA TSUPREM-4 P-channel GAA
option device=X
$ Specify x mesh
LINE X LOCATION=0 SPACING=0.5 TAG=LEFT
LINE X LOCATION=1.5 SPACING=0.2
LINE X LOCATION=2.5 SPACING=0.2
LINE X LOCATION=3.5 SPACING=0.3 TAG=RIGHT

$ Specify y mesh
$LINE Y LOCATION=0  SPACING=0.01 TAG=OXTOP
LINE Y LOCATION=0.03 SPACING=0.006 TAG=OXBOTTOM
LINE Y LOCATION=2.0 SPACING=1.0 TAG=SIBOTTOM

$ELIMINATE COLUMNS X.MIN=1.8 X.MAX=5.2 Y.MIN=0.05
$ELIMINATE COLUMNS Y.MIN=0.03

$ Define isolation oxide and silicon substrate
$REGION  OXIDE XLO=LEFT XHI=RIGHT YLO=OXTOP  YHI=OXBOTTOM
REGION  SILICON XLO=LEFT XHI=RIGHT YLO=OXBOTTOM YHI=SIBOTTOM
INITIALIZE <100> arsenic=1E20
deposit oxide thickness=0.03 spaces=6

$ Deposit epi with nonuniform vertical grid spacing
DEPOSIT SILICON BORON=1E14 THICKNESS=0.08 SPACES=10
$DEPOSIT SILICON BORON=1E17 THICKNESS=0.1 SPACES=5 DY=0.01
```

```
$ Plot initial mesh
SELECT  Z=1 TITLE="Initial Mesh"
PLOT.2D GRID Y.MAX=1 C.GRID=2
$PRINT.1D X.VALUE=0.0 LAYERS

$ Use vertical oxidation model to grow pad oxide
$METHOD  VERTICAL GRID.OXI=4
$DIFFUSE TIME=26 TEMP=1000 DRYO2

$SELECT  Z=1
$PRINT.1D X.VALUE=0.0 LAYERS
$etch oxide all
$select z=1
$print.1D x.value=1 layers

$gate oxide

$method vertical grid.oxi=4
diffuse time=43 temp=950 dryo2

select z=1

implant boron dose=2e12 energy=20
diffuse time=10 temp=950 dryo2
diffuse time=60 temp=800 inert
print.1D x.value=1 layers

$ Deposit, dope, and pattern poly
DEPOSIT POLY THICK=0.5 SPACES=3
implant phosphorus dose=5e15 energy=100
DIFFUSE TIME=120 TEMP=800 inert
ETCH  POLY LEFT P1.X=2
etch oxide left P1.x=2
plot.2D boundary

$ Source/drain implant and anneal
IMPLANT boron DOSE=2E15 ENERGY=25
diffuse time=30 temp=800 dryO2
DIFFUSE TIME=180 TEMP=800
$ Metallization
DEPOSIT OXIDE THICK=0.4
ETCH  OXIDE LEFT P1.X=1.0 P2.X=1.1 P1.Y=-2 P2.Y=0.0
DEPOSIT ALUMINUM THICK=1
ETCH  ALUMINUM RIGHT P1.X=1.2 P2.X=1.3 P1.Y=-3 P2.Y=2

$ Reflect structure, then save complete MOSFET
STRUCTURE OUT.FILE=S4EX9S1
STRUCTURE REFLECT RIGHT
select z=1
plot.2d boundary x.min=0 x.max=7 y.min=-0.6 y.max=0.1

STRUCTURE OUT.FILE=gaapout PISCES

$ Plot grid & profiles for complete structure
SELECT  Z=DOPING TITLE="SOI MOSFET"
PLOT.2D Y.MAX=0.1 y.min=-0.2
$COLOR  SILICON COLOR=7
$COLOR  OXIDE  COLOR=5
COLOR  POLY  COLOR=3
COLOR  ALUMINUM COLOR=2
FOREACH X ( 16 TO 21 STEP 1 )
 CONTOUR VALUE=( 10^ X ) COLOR=4 LINE.TYP=2
```

```
 CONTOUR VALUE=(-(10^ X )) COLOR=2 LINE.TYP=5
END
PLOT.2D ^AX ^CL

PLOT.2D boundary SCALE Y.MAX=1 C.GRID=2

$ Plot 1D concentration profiles
SELECT  Z=LOG10(ACTIVE(BORON)) TITLE="Doping Profiles" +
  LABEL="log(Active Concentration)"
PLOT.1D X.VALUE=1 BOTTOM=15 TOP=21 LEFT=-0.1 RIGHT=0 LINE.TYP=5 +
  COLOR=2
LABEL  LABEL="Boron (x=1)" X=-0.1 Y=17

SELECT  Z=LOG10(ACTIVE(boron))
PLOT.1D X.VALUE=3.4 ^AXES ^CLEAR LINE.TYP=2 COLOR=3
LABEL  LABEL="Arsenic (x=0)" X=-0.1 Y=20.3

$ Plot 1D concentration profiles
SELECT  Z=LOG10(ACTIVE(BORON)) TITLE="Doping Profiles" +
  LABEL="log(Active Concentration)"
PLOT.1D y.VALUE=-0.01 BOTTOM=15 TOP=21 LEFT=0 RIGHT=6 LINE.TYP=5 +
  COLOR=2
LABEL  LABEL="Boron (x=1)" X=-0.1 Y=17

SELECT  Z=LOG10(ACTIVE(ARSENIC))
PLOT.1D X.VALUE=0 ^AXES ^CLEAR LINE.TYP=2 COLOR=3
LABEL  LABEL="Arsenic (x=0)" X=-0.1 Y=20.3
```

MEDICI Simulation file, p-channel GAA

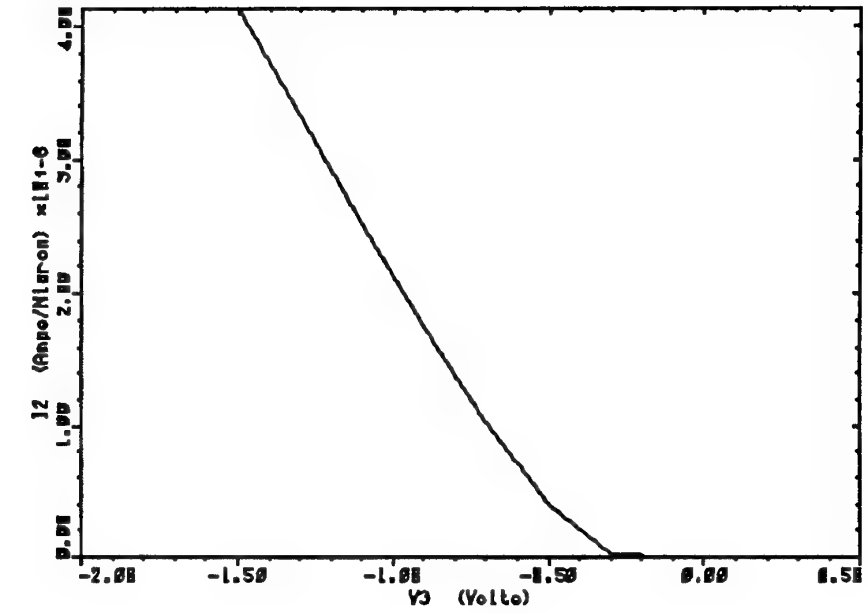
```
$option device=X
mesh infile=gaapout tsuprem4 elec.bot poly.ele
$ comment electrodes source=1 gate=3 drain=2 substrate=4
contact number=3 n.poly
interfac qf=1.5e11
$plot.2d junction boundary y.max=0.1 y.min=-0.15 x.min=0 x.max=7
$plot.1d doping x.start=0 x.end=7 top=1e20 bottom=1e14 y.start=-0.07
$+ y.end=-0.07 Y.logari
$models conmob consrh bgn prpmob
$material silicon n.ioniza=1e6 ecn.ii=2.54e6 taup0=2e-8
symb carriers=0
solve v3=0 v2=0.5 V4=0 V1=0 init
$plot.2d boundary depletio y.max=0.01 y.min=-.15
$stop
symb carriers=1 holes newton
method autonr
solve out.file=n2init
solve v2=0.05 v3=0.5 v4=0.5 init
log ivfile=gaapvt
solve pro v1=0 v2=0.1 V4=0.5 v3=0.5 elec=(3,4) vstep=-0.2 nstep=10
plot.1D x.axis=V3 y.axis=I2 left=-2 right=0.5 bot=0 absolute
plot.1d x.axis=V3 y.axis=I2 left=-2 right=0.5 y.logari absolute
+ bot=1e-14 top=1e-4
stop
$load in.file=n2init
models conmob consrh bgn prpmob impact.i
symb carriers=2 newton
$solve v1=0 v2=0 v3=0 v4=0 pre
$solve v1=0 v2=0 v3=1 v4=0 pre out.file=n2init
$log ivfile=n2vd1
$solve v1=0 v2=0 v3=1 v4=0 pro elec=2 vstep=0.2 nstep=25
```

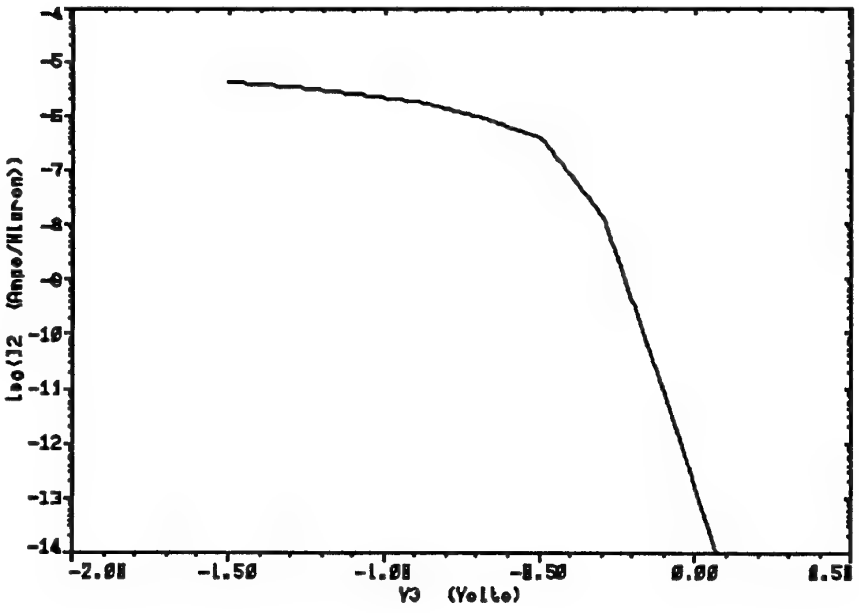
```
$plot.1D x.axis=v2 y.axis=i2 left=0 right=5 bot=0

$load in.file=n2init
$solve v1=0 v2=0 v3=2 v4=0 pre out.file=n2init
$log ivfile=n2vd2
$solve v1=0 v2=0 v3=2 v4=0 pro elec=2 vstep=0.2 nstep=25
$plot.1d x.axis=v2 y.axis=i2 left=0 right=5 bot=0

$load in.file=n2init
$solve v1=0 v2=0 v3=3 v4=0 pre out.file=n2init
$log ivfile=n2vd3
$solve v1=0 v2=0 v3=3 v4=0 pro elec=2 vstep=0.2 nstep=25
$plot.1d x.axis=v2 y.axis=i2 left=0 right=5 bot=0

$load in.file=n2init
$solve v1=0 v2=0 v3=4 v4=0 pre out.file=n2init
$log ivfile=n2vd4
$solve v1=0 v2=0 v3=4 v4=0 pro elec=2 vstep=0.2 nstep=25
$plot.1d x.axis=v2 y.axis=i2 left=0 right=5 bot=0

$load in.file=n2init
$solve v1=0 v2=0 v3=5 v4=0 pre
$log ivfile=n2vd5
$solve v1=0 v2=0 v3=5 v4=0 pro elec=2 vstep=0.2 nstep=25
$plot.1d x.axis=v2 y.axis=i2 left=0 right=5 bot=0


solve v1=0 v2=0 v3=0 v4=0 pre
solve v1=0 v2=0 v3=0 v4=-1 pre
solve v1=0 v2=0 v3=0 v4=-2 pre
solve v1=0 v2=0 v3=0 v4=-3 pre
solve v1=0 v2=0 v3=0 v4=-4 pre
solve v1=0 v2=0 v3=0 v4=-5 pre out.file=n2init
solve v1=0 v2=0 v3=1 v4=-5 pre out.file=n2init
$log ivfile=n2vd1-5
$solve v1=0 v2=0 v3=1 v4=-5 pro elec=2 vstep=0.2 nstep=25
$plot.1d x.axis=v2 y.axis=i2 left=0 right=5 bot=0

$load in.file=n2init
solve v1=0 v2=0 v3=2 v4=-5 pre out.file=n2init
$log ivfile=n2vd2-5
$solve v1=0 v2=0 v3=2 v4=-5 pro elec=2 vstep=0.2 nstep=25
$plot.1d x.axis=v2 y.axis=i2 left=0 right=5 bot=0

$load in.file=n2init
solve v1=0 v2=0 v3=3 v4=-5 pre out.file=n2init
$log ivfile=n2vd3-5
$solve v1=0 v2=0 v3=3 v4=-5 pro elec=2 vstep=0.2 nstep=25
$plot.1d x.axis=v2 y.axis=i2 left=0 right=5 bot=0

load in.file=n2init
solve v1=0 v2=0 v3=3.5 v4=-5 pre out.file=n2init
solve v1=0 v2=0 v3=4 v4=-5 pre out.file=n2init
log ivfile=n2vd4-5
solve v1=0 v2=0 v3=4 v4=-5 pro elec=2 vstep=0.2 nstep=25
plot.1d x.axis=v2 y.axis=i2 left=0 right=5 bot=0

load in.file=n2init
solve v1=0 v2=0 v3=4.5 v4=-5 pre out.file=n2init
solve v1=0 v2=0 v3=5 v4=-5 pre out.file=n2init
log ivfile=n2vd5-5
solve v1=0 v2=0 v3=5 v4=-5 pro elec=2 vstep=0.2 nstep=25
plot.1d x.axis=v2 y.axis=i2 left=0 right=5 bot=0
```

4.4. Modelling results

4.4.1. P-channel devices

channel doping=boron15 keV	Vth(V)
1e11	-0.9
1e12	-0.45
2e12	+0.1

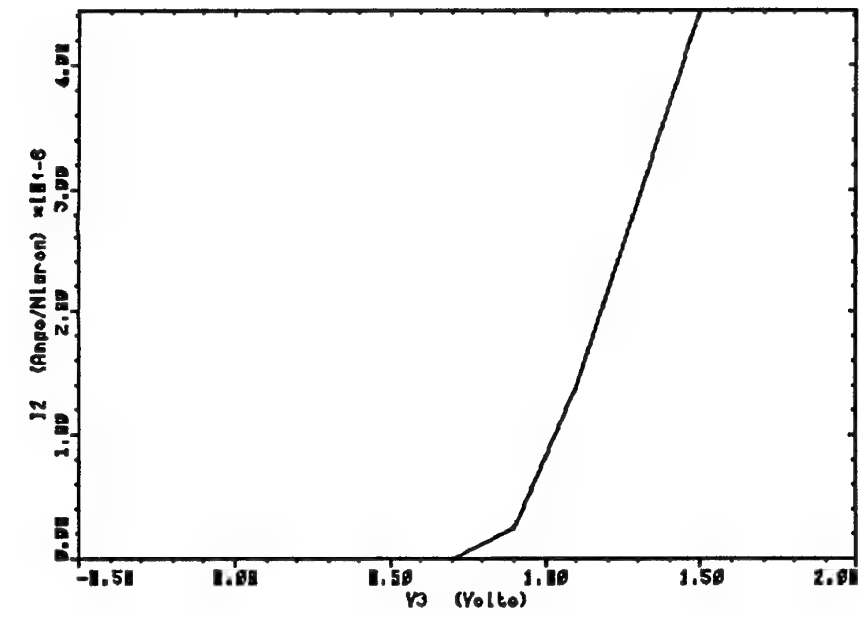


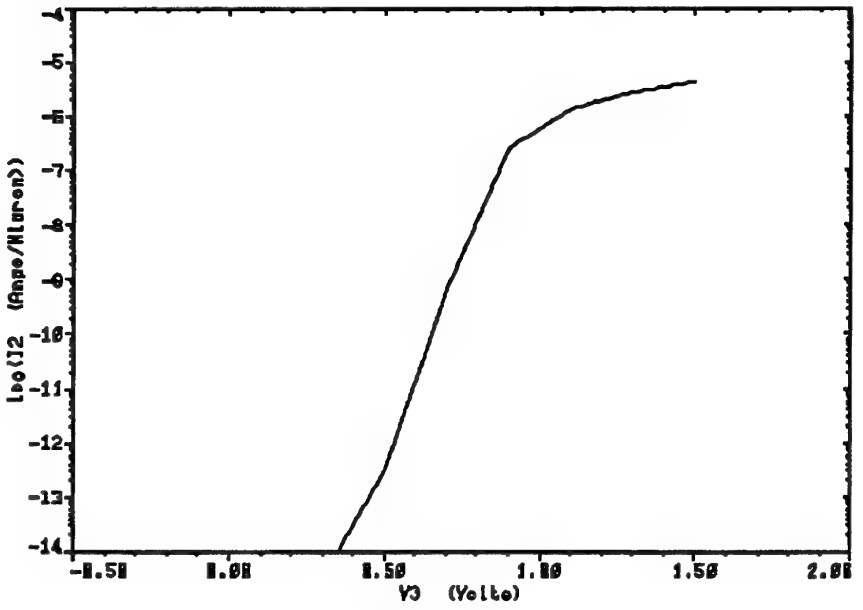


Curves for dose=1e12

4.4.2.N-channel devices

Vth boron dose (15 keV)	Vth (V)
8e11	0.1
2e12	0.65
2.5e12	0.9
3e12	1.1





curves for dose=2.5e12

4.5. Process run sheet

The spreadsheet below describes the process steps and process splits for the fabrication of the devices.

	Operations	Time	Thickness	rum. C	rum. E	rum. G	rum.M	B22	B23	S45	S46	S47	E48	E49	E50	G51	G52	G53	M54	M55	M56
1	Prometrix			2000 A	2000 A	2000 A	2000 A														
2	Clean																				
3	Oxidation C33 950°C	xxx	1000 A	1560 A	1560 A	1560 A	1560 A														
4	Oxide strip BHF		1000 A																		
5	Prometrix																				
6	Clean																				
7	Oxidation C33 950°C	0h:55'	400 A	1384 A	1348 A	1384 A	1384 A														
8	Oxide strip BHF		400 A																		
9	Prometrix																				
10	Clean																				
11	Oxidation C33 950°C	0h:40'	300 A	1252 A	1252 A	1252 A	1252 A														
12	Oxide strip BHF		300 A																		
13	Prometrix																				
14	Oxidation C33 950°C	0h:40'	300 A	1120 A	1120 A	1252 A	1252 A														
15	Oxide strip BHF		300 A																		
16	Prometrix																				
17	Clean																				
18	Pad oxidation C33 950°C	0h:40'	300 A	988 A	988 A	1120 A	1120 A														
19	Nitride deposition 800°C	0h:64'	2000 A																		
20	Pre-clean																				
21	Degassing O2 950°C	0h:15'																			
22	Photolitho 1 (Active area)	New mask																			
22a	Photolitho 1 (Active area)	Old mask																			
23	Nitride etch ET 340																				
24	Resist strip																				
25	Clean																				
26	Degassing N2 950°C	0h:10'																			
27	Photolitho 2 (field impl)	New mask																			
27a	Photolitho 2 (field impl)	Old mask																			
28	Implantation P (Boron)	30 Kev	1,00E+14																		
29	Resist strip																				
30	Oxide etch BHF		300 A																		
31	Clean																				
33	Diffusion N2 950°C	0h:45'																			
34	Silicon etch RIE																				
35	Clean																				
36	Wet oxidation 950°C	1h:00'																			
37	Oxinitride etch BHF BHF	0":20"																			
38	Nitride strip H3PO4 170°C																				
39	Oxide etch BHF		300 A																		
40	Clean																				
41	Degassing N2 950°C	0h:15'																			
42	Photolitho 3 (cavity)	New mask																			
42a	Photolitho 3 (cavity)	Old mask																			
43	Cavity etch BHF		18000 A																		
44	Resist strip H2SO4																				
45	Clean																				
46	Gate oxidation 950°C	62 min	300 A	856 A	856 A	856 A	856 A														
47	Photolitho 4 (n-ch VTH)	New mask																			
	Photolitho 4 (n-ch VTH)	Old mask																			
47a	N-channel implant																				
	Boron 1.5e12, 20 keV																				
	Boron 1.7e12, 20 keV																				
	Boron 2e12, 20 keV																				
	Boron 2.5e12, 20 keV																				
	Boron 2.7e12, 20 keV																				
	Boron 3e12, 20 keV																				
	Boron 3.5e12, 20 keV																				
	Boron 4e12, 20 keV																				
	Boron 4.2e12, 20 keV																				
49	Resist strip H2SO4																				
50	clean, no HF																				
51	Degassing Ar 800°C	0h:30'																			
52	Photolitho 5 Vt PMOS	New mask																			
52a	Photolitho 5 Vt PMOS	Old mask																			
53	P-channel implant																				
	Phos 1e11, 60 keV																				
	Phos 3e11, 60 keV																				
	Phos 5e11, 60 keV																				
	Boron 2e11, 20 keV																				
	Boron 3e11, 20 keV																				
	Boron 4e11, 20 keV																				
	Boron 1.2E12, 20 keV																				
	Boron 1e12, 20 keV																				
	Boron 8E11, 20 keV																				
54	Resist strip																				
55	Pre-clean																				
56	Clean, no HF																				
57	Additional gate oxidation s	0h:10'	With Ar anneal 800°C, 60 min.																		
58	Poly deposition 625°C		4000 A																		
59	N-Implant (Phos) poly gate	100 Kev, 1e16																			
60	Pre-clean																				
61	Clean																				
62	Diffusion Ar 800°C	2h:00'																			

63	Photolitho 6 gate	New mask		
63a	Photolitho 6 gate	Old mask		
64	poly etch RIE + 20 sec etch SF6			
46a	Resist strip			
65	Oven 140°C			
66	Photolitho 7 (S&D PMOS	New mask		
66a	Photolitho 7 (S&D PMOS	Old mask		
67	P-Implant (Boron) S&D 20 Kev, 4E+15			
68	Resist strip			
69	Pre-clean			
70	Clean, no HF			
71	Degassing N2 400°C	0h:30'		
72	Photolitho 8 (S&D NMOS	New mask		
	Photolitho 8 (S&D NMOS	Old mask		
73	N-Implant (As) 40 keV, 4E+15			
74	Pre-clean			
75	Resist spin, front of wafer			
76	Backside poly etch			
77	Resist strip			
78	Clean			
79	S&D reox 800°C	0h:30'		
80	Argon anneal 800°C	3h:00'		
81	Deposit undoped pyrox (5000 A)			
82	Densification O2 800°C	0h:30'		
83	Photolitho 9 (contact)	New mask		
83a	Photolitho 9 (contact)	Old mask		
84	Pyrox etch BHF			
85	Resist strip			
86	Clean			
87	Metal deposition Al/Si		10000 A	
88	Photolitho 10 (Alum)	New mask		
88a	Photolitho 10 (Alum)	Old mask		
89	Aluminium etch			
90	Resist strip HNO3			
91	Contact testing			
92	Sintering in forming gas 4:	0h:30'		
93	Undoped Pyrox deposition	5':30"	3000 A	
94	Photolitho 11 (Vias)	New mask		
94	Photolitho 11 (Vias)	Old mask		
95	Pyrox etch	3':05"		
96	Resist strip HNO3			
97	Backside oxide strip HF			
98	The end			

Process steps and process splits for the fabrication of the devices. "B" wafers are bulk monitor wafers; "S" wafers are for regular SOI devices; "E" wafers are for regular SOI devices, but for high-temperature applications; "G" wafers are for GAA devices with the MPCMAY93 "new" mask set; "M" wafers are for GAA devices with the MPCJAN93 "old" mask set.

5. Measurement results

5.1. Pre-rad measurements

The following curves present the electrical characteristics of:

1- GAA transistors (all devices have a width of 3 μm and a length of 3 μm).

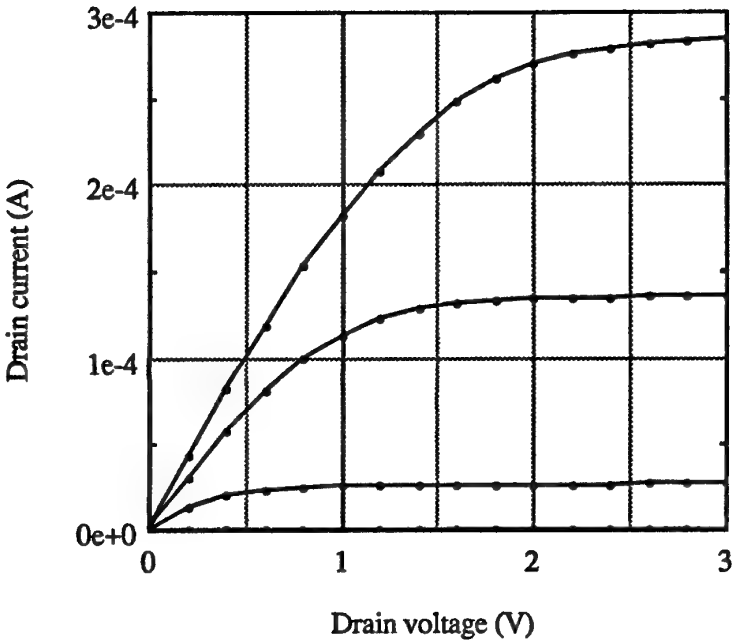
2- GAA CMOS inverters and output buffers

3- GAA CMOS 64 kbit SRAM

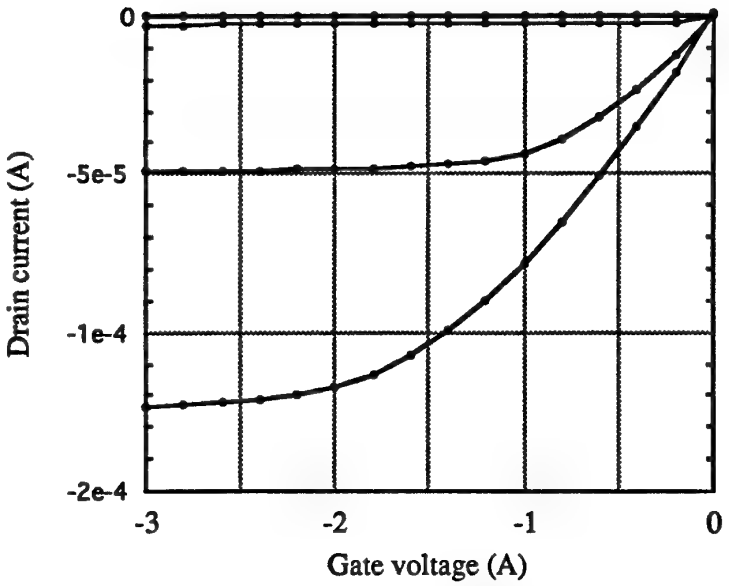
These devices are similar to the packaged devices supplied with the present report.

Three fabrication runs were processed in 1993. These are: run 193 (processed in February 93), run 493 (processed in May 93) and run 693 (processed in June 93). The two first runs exhibited uncontrolled gate leakage and sometimes source-to-drain leakage in those devices which used mesa isolation (among which the GAA devices). At first glance it seemed to be a gate oxide punchthrough effect, but after more thorough analysis we discovered that the leakage originated from a poly stringer problem along the edge of the devices. This problem was not observed in previous runs where an "old" SF6 plasma etcher was used to pattern the gates. Since early 1993 we have been using a chlorine-based RIE reactor for gate etching. The good anisotropy of the process had left poly along the edge of the devices, yielding leakage problems. In run 693 we modified the gate etch procedure and included some isotropic etch after the anisotropic gate etch, which solved the problem. All the devices described in the following pages come from run 693.

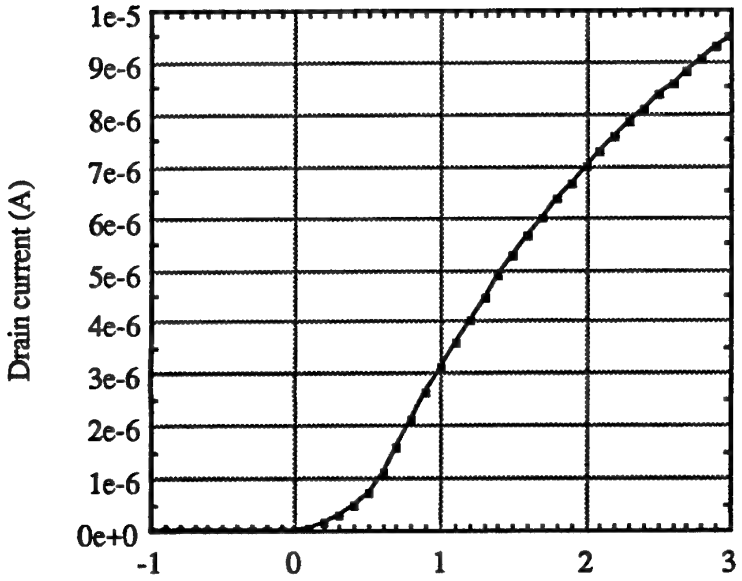
5.1.1. Transistors



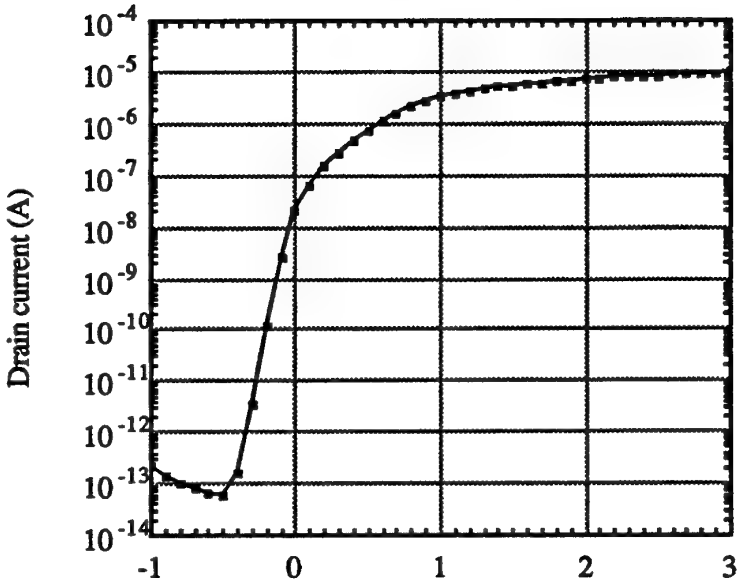
Id(Vd) of a 3μmx3μm n-channel GAA device. Vg=0, 1, 2 and 3 V



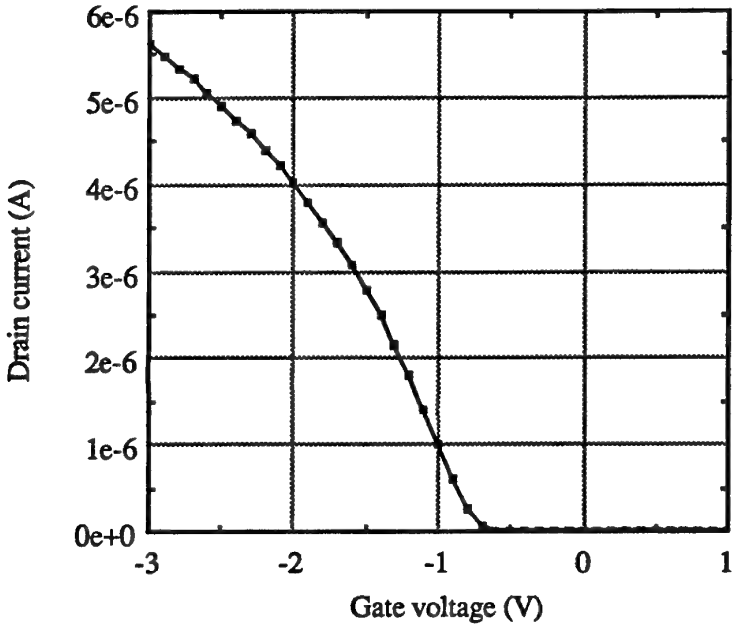
Id(Vd) of a 3μmx3μm p-channel GAA device. Vg=0, -1, -2 and -3 V



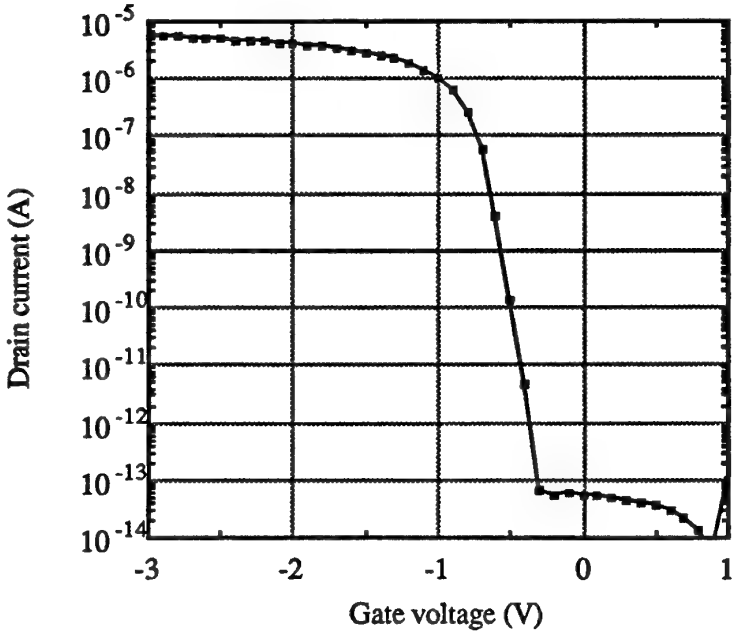
Id(Vg) (linear scale) of a 3μmx3μm GAA n-channel device



Id(Vg) (log scale) of a 3μmx3μm GAA n-channel device

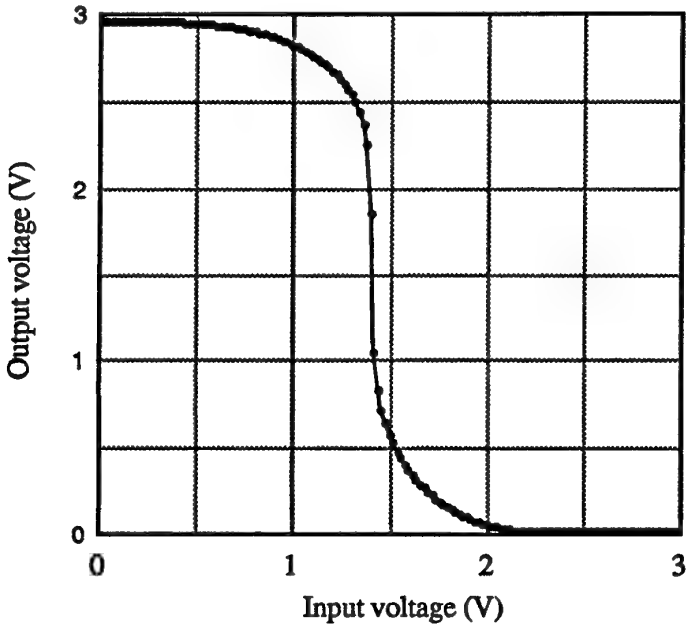


Id(Vg) (linear scale) of a 3μmx3μm GAA p-channel device

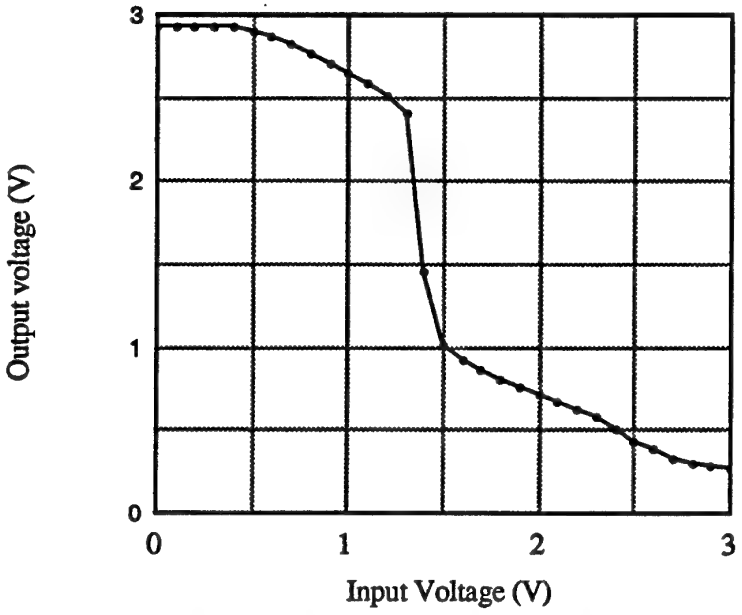


Id(Vg) (log scale) of a 3μmx3μm GAA p-channel device

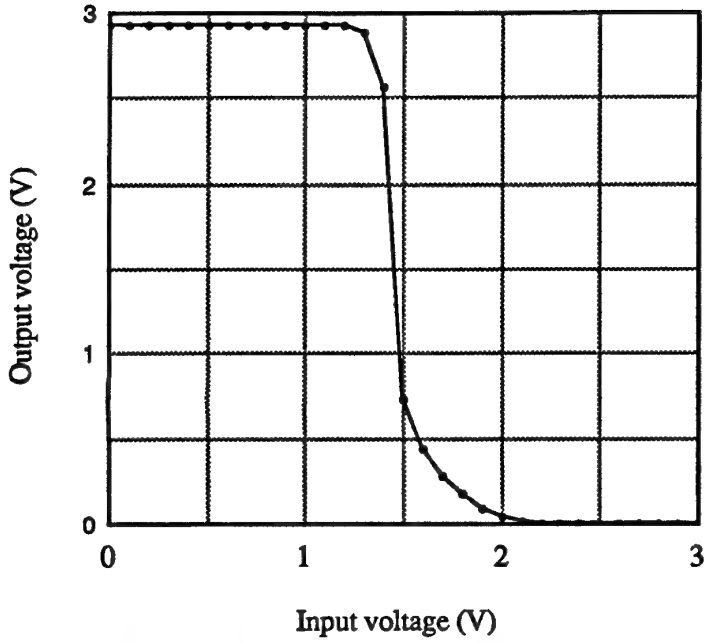
5.1.2. Inverters and output buffers



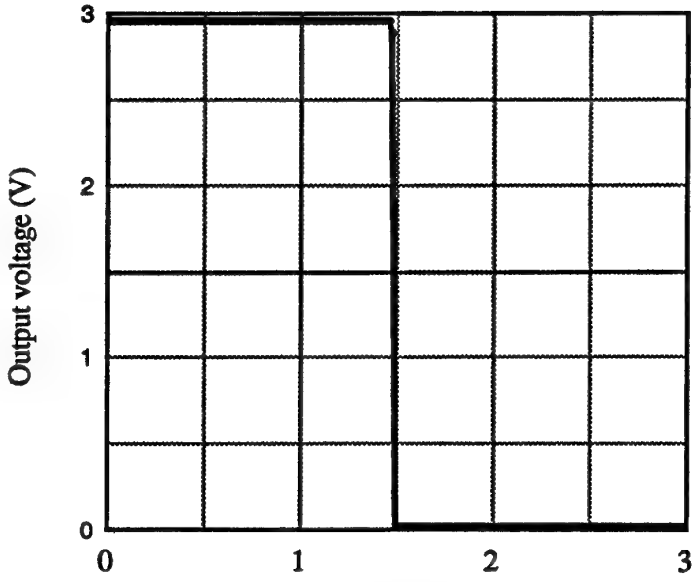
Measured transfer characteristic of a regular GAA CMOS inverter



Measured transfer characteristic of a GAA CMOS inverter with diode pair (see pages 32 and 33 for layout and simulated characteristics).



Measured transfer characteristic of a GAA CMOS inverter with pull-up configuration (see page 32 for layout and simulated characteristics).



Measured transfer characteristic of a GAA CMOS output buffer

5.1.3. 64-bit SRAM

Let us remind that, in order to find out the best memory cell design, every single of the 64 bits of the SRAMS has a design different from the other bits (different W/L ratios). This may yield non-functional bits on every memory chip, but will also indicate which is the best design which has to be repeated to obtain fully functional GAA SRAMs in the future. The SRAMs were tested by writing a chess-board pattern in the cells and then reading it. As shown in the figure below, all cells are functional, with the exception of four of them. We are currently investigating whether these non-functional cells are so because of a design error or because a default in the masks. As it was said before, all memory cells are different. The figure below indicates the particularity of each cell in terms of number of p-channel devices in each half memory cell (which, times 3 μm, yields the width of the equivalent p-channel transistor), the type of write cell, and the amount of pass transistors.

WRITE ↓	P-ch transistors in half memory cell → READ ↓								# of pass transistors
	3	4	5	6	7	8	9	10	
Write n	X	X	X	X	?	X	X	?	3
Write n	X	X	X	X	X	X	X	X	4
Write n w precharge	X	X	X	X	?	X	X	X	3
Write n w precharge	X	X	X	X	X	X	X	X	4
Write n tristate	X	X	X	X	?	X	X	X	3
Write n tristate	X	X	X	X	X	X	X	X	4
Write n tristate w precharge	X	X	X	X	X	X	X	X	3
Write n tristate w precharge	X	X	X	X	X	X	X	X	4

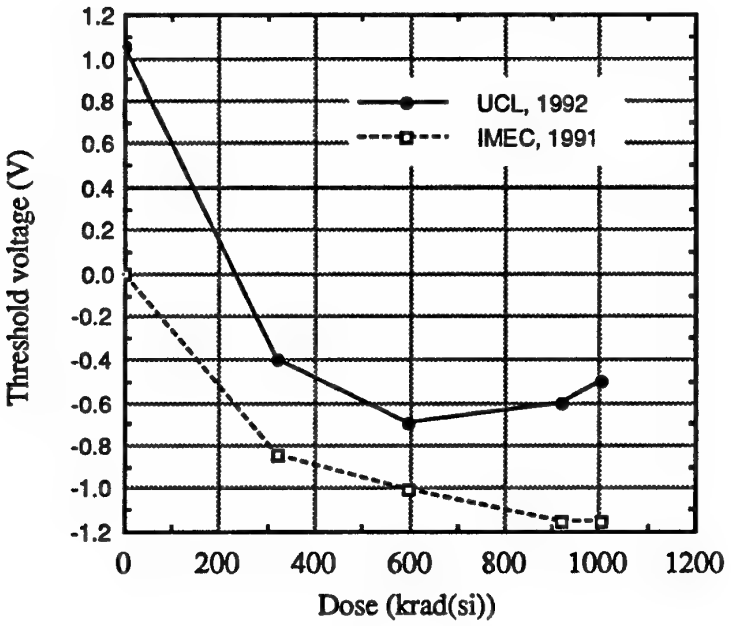
Tested 64-bit SRAM. "X"=functional cells; "?"= non-functional cells.

The access time of the memories @ V_{dd}=3V is approximately 8 μs (the same memories made in SOI, not GAA) have an access time of 150 ns). The difference might be due to the high capacitive coupling between the gate and the other device terminals in GAA transistors. The current consumption of the devices @ V_{dd}=3V is 300 μA.

5.2. Irradiation results

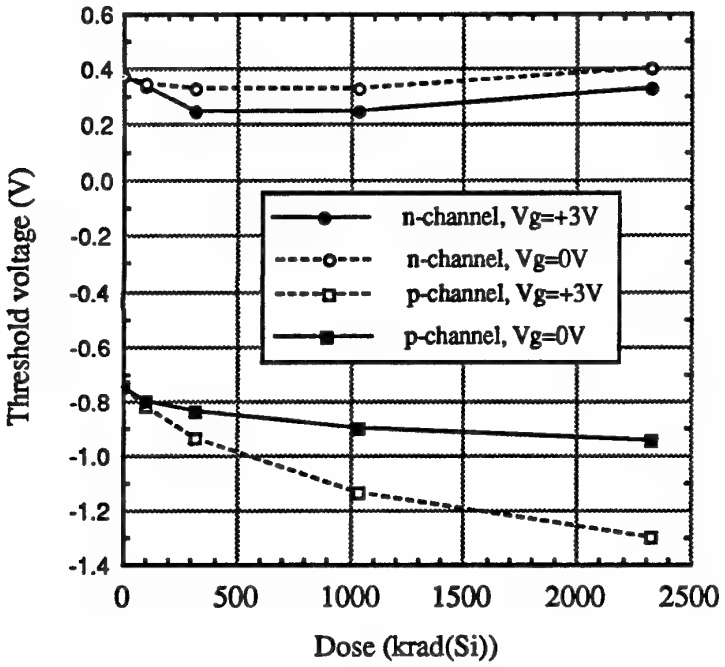
5.2.1. Transistors

In order to recall "where we come from", we shall first present results of irradiation carried out on "old" GAA devices (fabricated at UCL in 1992) and on "older" devices fabricated at IMEC in 1991. The graph below presents the threshold voltage vs. the irradiation dose in those devices (n-channel devices, irradiated at V_G=+3V).

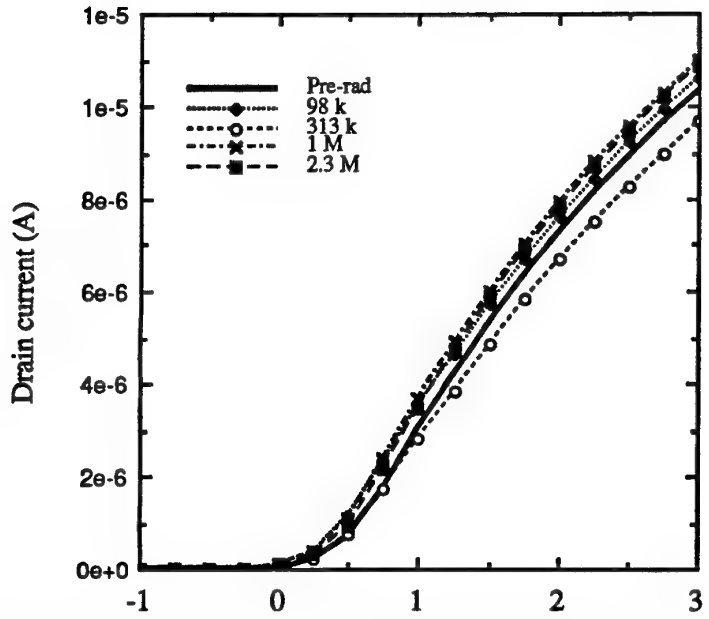


Threshold voltage vs. dose (^{60}Co) in "old" n-channel GAA devices (made before this program started).

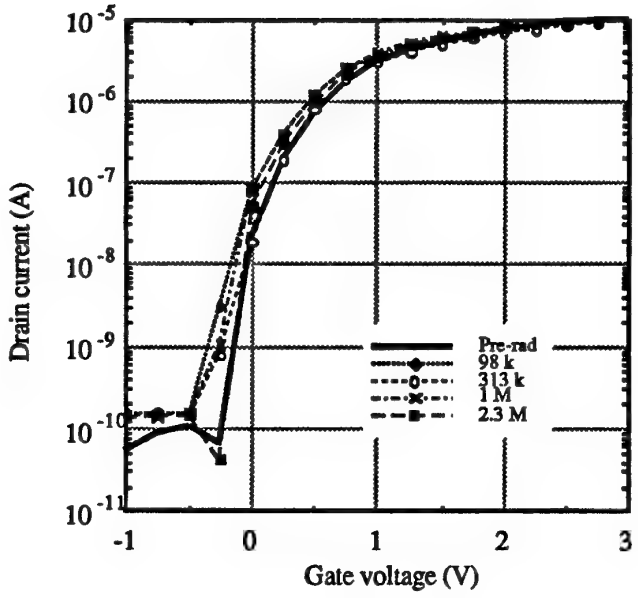
The new devices (with a gate oxide thickness of 30 nm) have a much better behavior. The curves below represent the evolution of threshold voltage with dose for two gate bias conditions. The dose-rate is 4 rad(Si) per second.



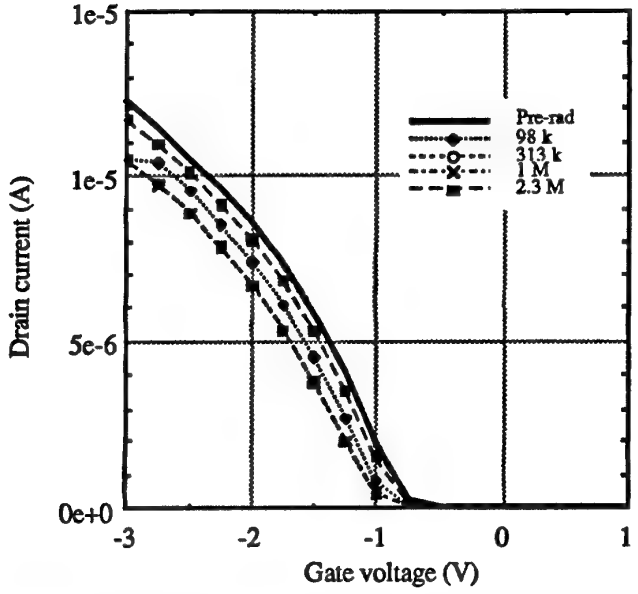
Threshold voltage vs. dose for n- and p-channel GAA devices, and for a gate voltage of 0 and +3 volts. The +3 V bias on the p-channel device occurs in some pass-gate configurations, in a real circuit, and it represents a worst-case situation.



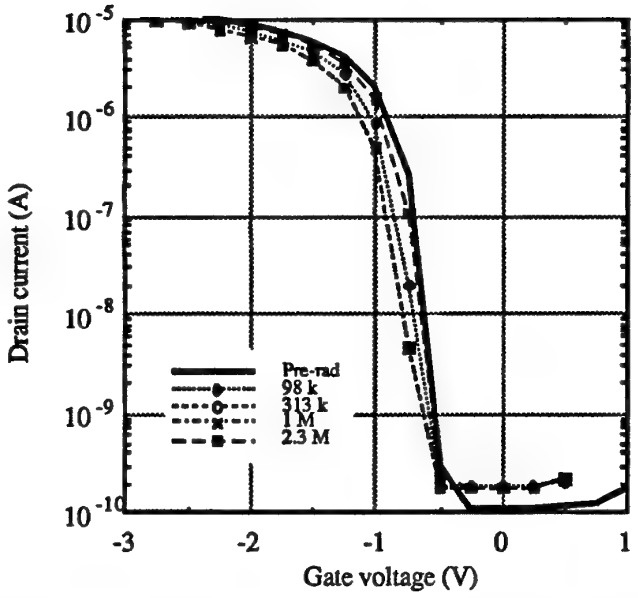
$I_D(V_G)$ in a 3μmx3μm GAA n-channel MOSFET for different irradiation doses (Pre-rad, 98 krad(si), 313 krad(si), 1034 krad(si), and 2324 krad(si)). V_G=+3V, V_S=0V and V_D=0V during the irradiation.



Log $I_D(V_G)$ in a 3μmx3μm GAA n-channel MOSFET for different irradiation doses (Pre-rad, 98 krad(si), 313 krad(si), 1034 krad(si), and 2324 krad(si)). V_G=+3V, V_S=0V and V_D=0V during the irradiation. Note the absence of edge leakage.



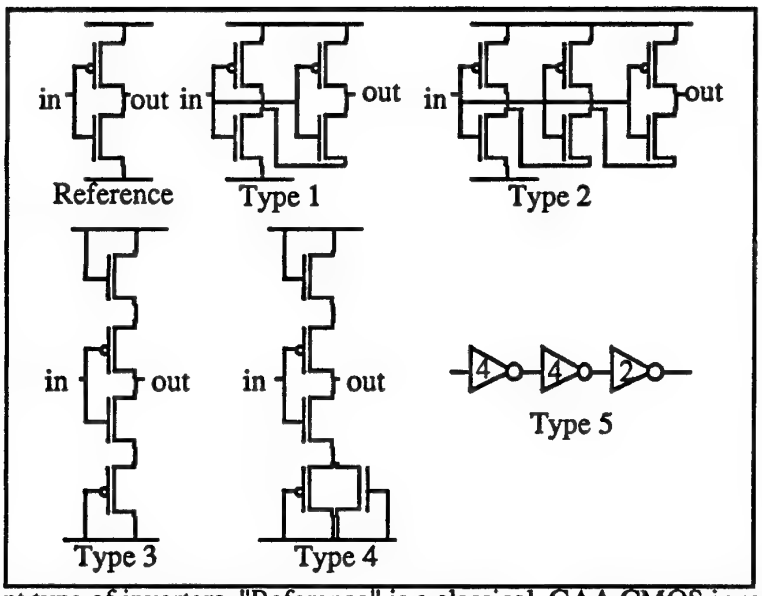
$I_D(V_G)$ in a 3μmx3μm GAA p-channel MOSFET for different irradiation doses (Pre-rad, 98 krad(si), 313 krad(si), 1034 krad(si), and 2324 krad(si)). V_G=+0V, V_S=0V and V_D=0V during the irradiation.



Log $I_D(V_G)$ in a 3μmx3μm GAA p-channel MOSFET for different irradiation doses (Pre-rad, 98 krad(si), 313 krad(si), 1034 krad(si), and 2324 krad(si)). V_G=+0V, V_S=0V and V_D=0V during the irradiation.

5.2.2. Inverters

Different types of GAA inverters were irradiated. The design of the different types is presented below.

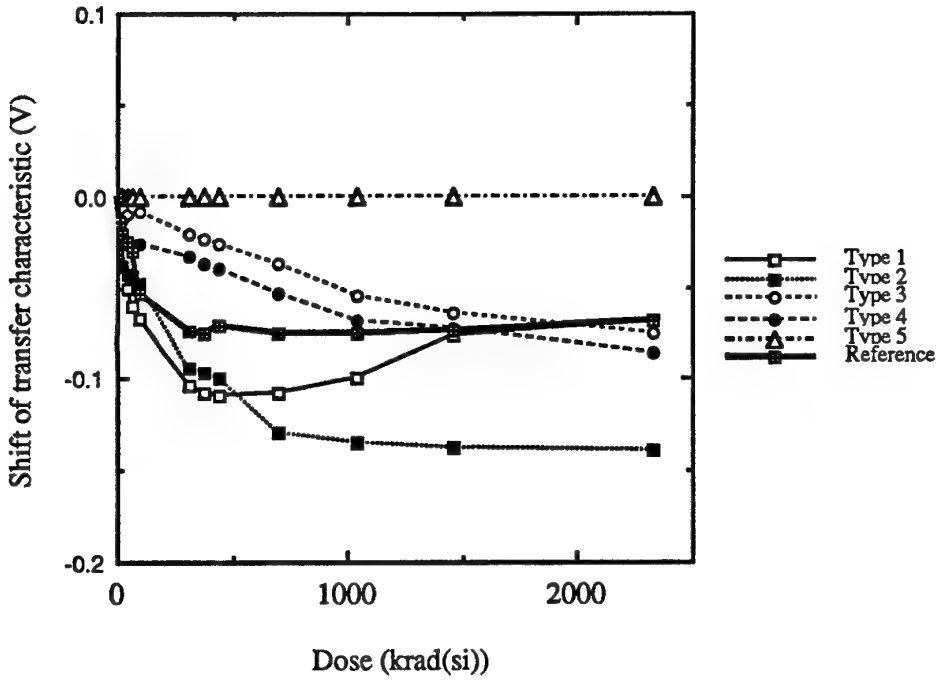


Different type of inverters. "Reference" is a classical GAA CMOS inverter. Types 1 and 2 are of "pull-up" type, Types 3 and 4 are of the "diode pair" type. Type 5 consists of 2 type-2 inverters in cascade with a type-4 inverter (buffer).

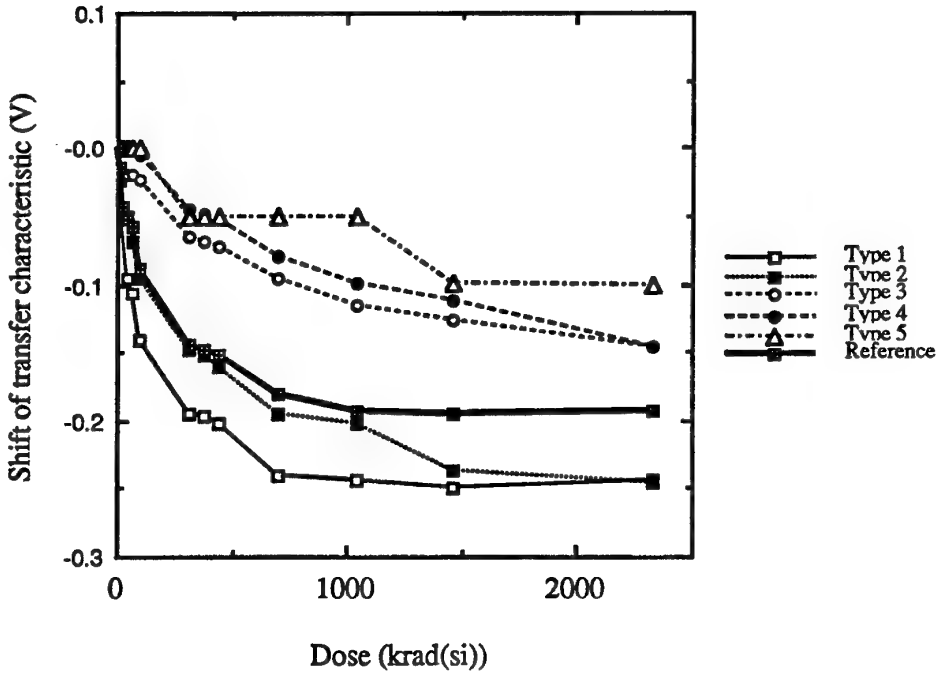
The shift of the transfer characteristic as a function of the dose was measured. Due to the negative shift of the threshold voltage of both n- and p-channel devices, all transfer characteristics shift to the left upon irradiation (see Figures below).

Due to the rather good behavior of the individual transistors, the shifts of the transfer characteristics of all inverters upon irradiation are quite modest (indeed, we expected threshold voltage shifts larger than one volt, but the observed shifts are smaller than 200 mV). The difference between the regular "reference" inverter and the other types of inverters is, therefore, not very spectacular. One can, nonetheless, appreciate the excellent radiation hardness of the type 5 inverter.

All inverters have been irradiated at the following ^{60}Co doses: 0 rad(si) (called "Pre-rad" in some Figure legends), 98 krad(si) (called "100k" in some Figure legends), 313 krad(si) (called "300k" in some Figure legends), 1034 krad(si) (called "1M" in some Figure legends), and 2324 krad(si) (called "2M" in some Figure legends).

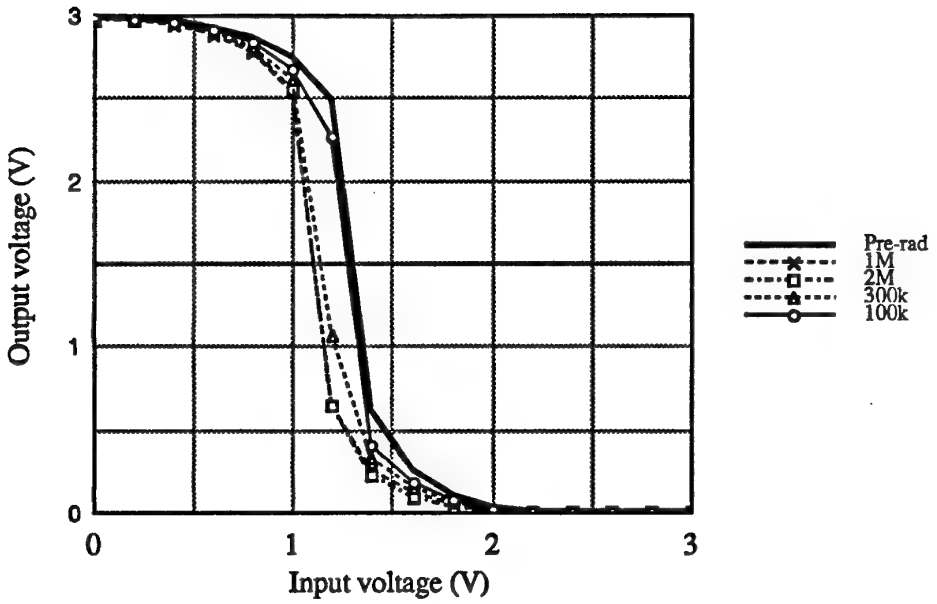


Shift of inverter transfer characteristic as a function of dose. Input voltage = 0 V during irradiation.

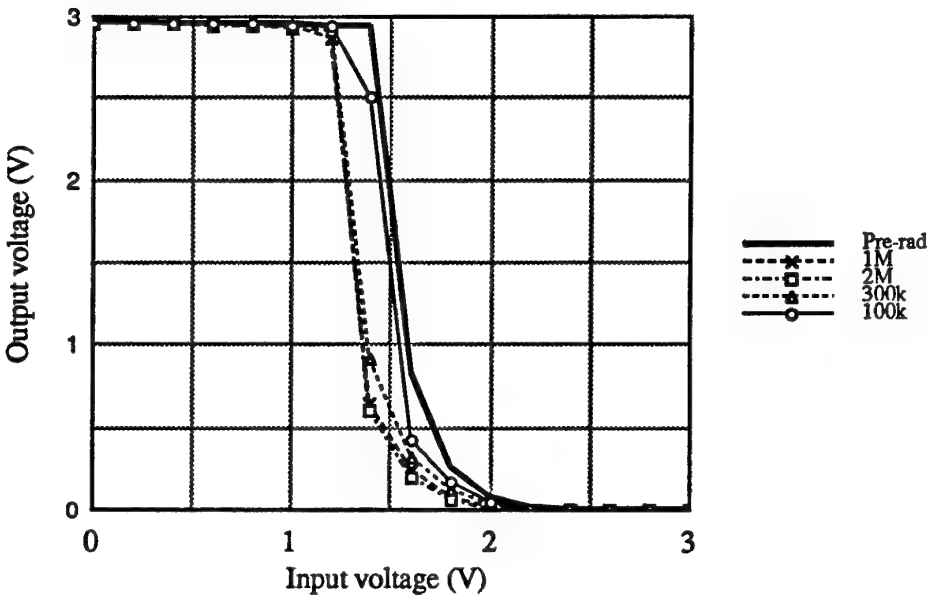


Shift of inverter transfer characteristic as a function of dose. Input voltage = +3 V during irradiation.

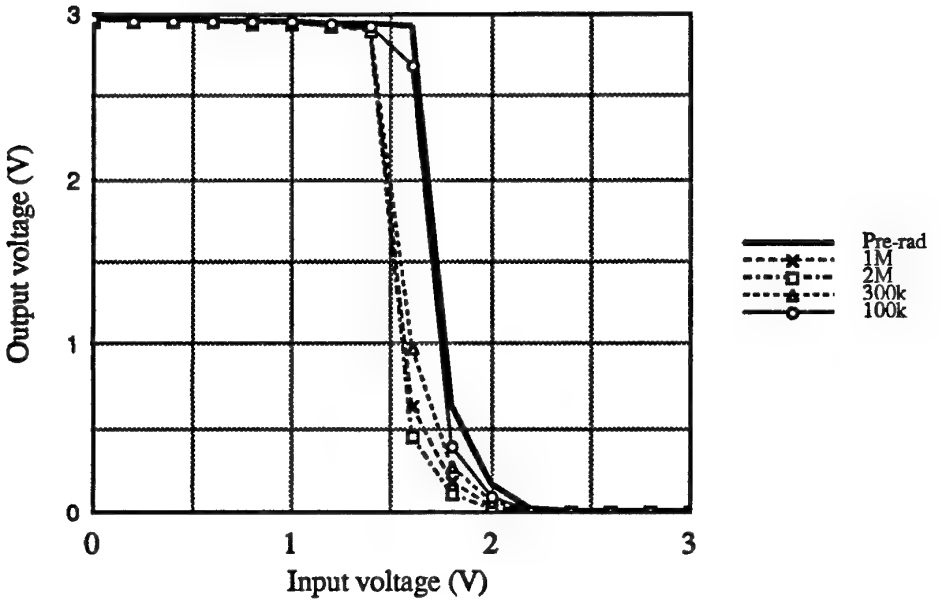
The transfer characteristics for different doses are presented in the Figures below.



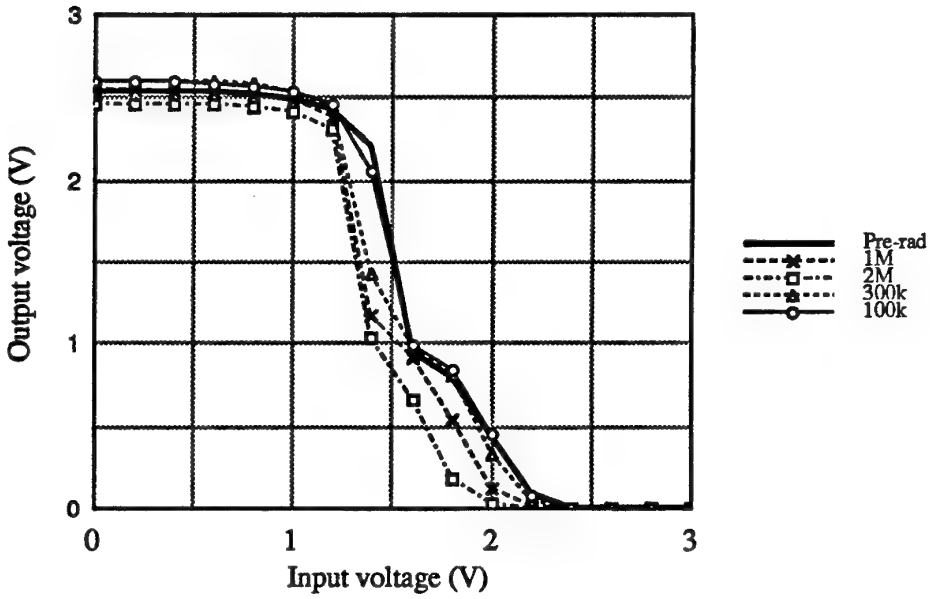
Reference inverter. Input voltage = +3 V during irradiation.



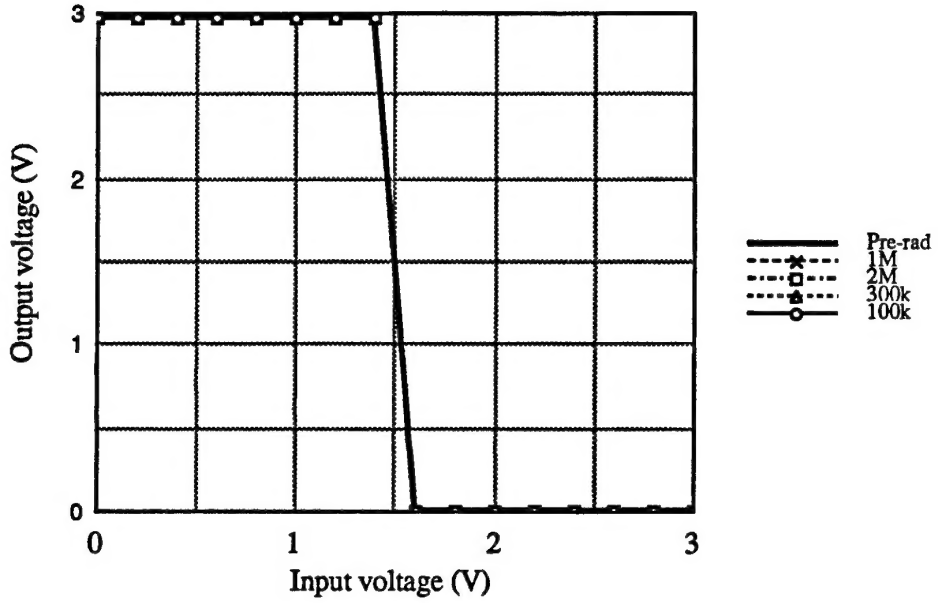
Type 1 inverter. Input voltage = +3 V during irradiation.



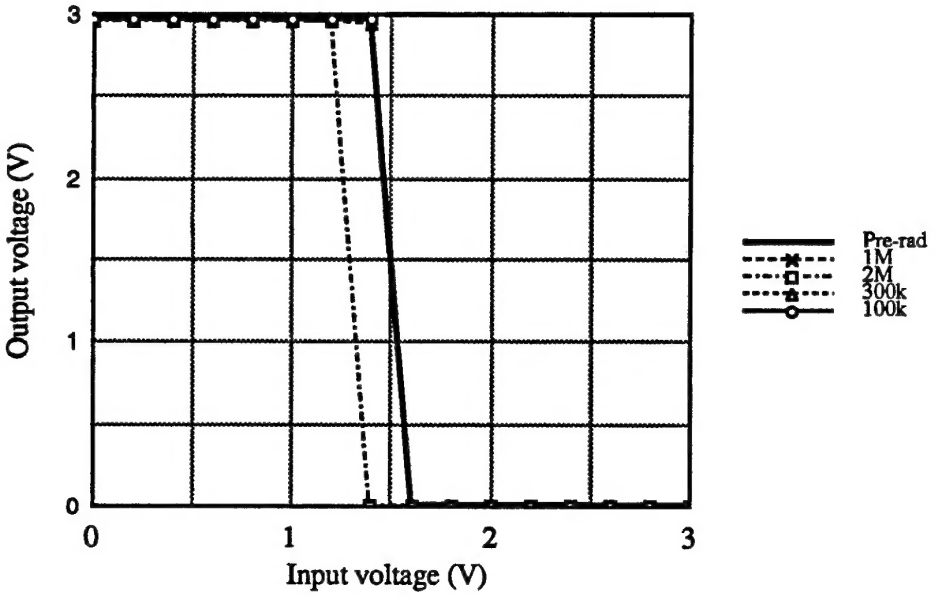
Type 2 inverter. Input voltage = +3 V during irradiation.



Type 3 inverter. Input voltage = +3 V during irradiation. The characteristics of type 4 inverters are similar to those of type 3 inverters.



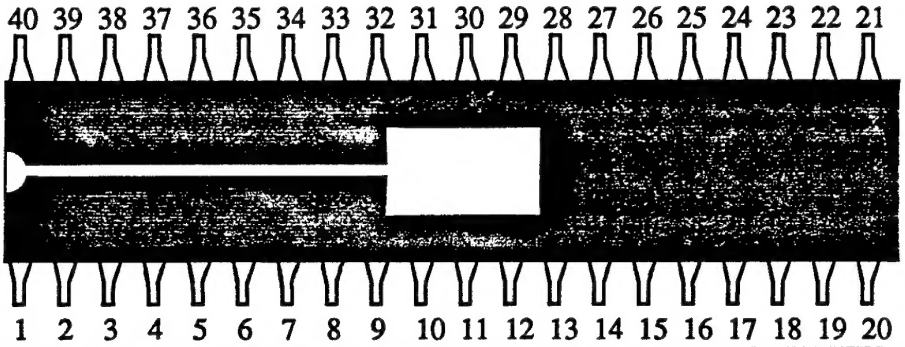
Type 5 inverter. Input voltage = 0 V during irradiation.



Type 5 inverter. Input voltage = +3 V during irradiation.

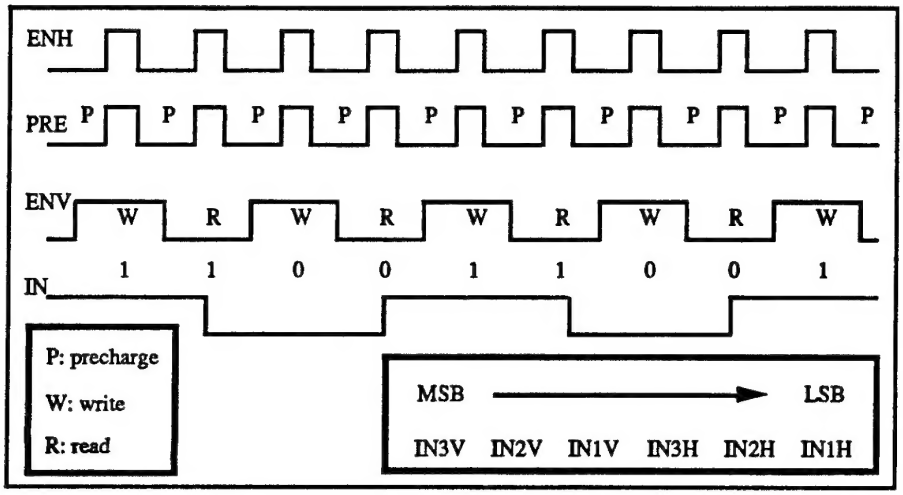
5.3. Packaged devices

Nine packaged devices are provided with this report. Five of them are labeled "G53" and contain an n-channel GAA device, a p-channel GAA transistor and a 64-bit GAA SRAM. The pin diagram of the packages is described below:

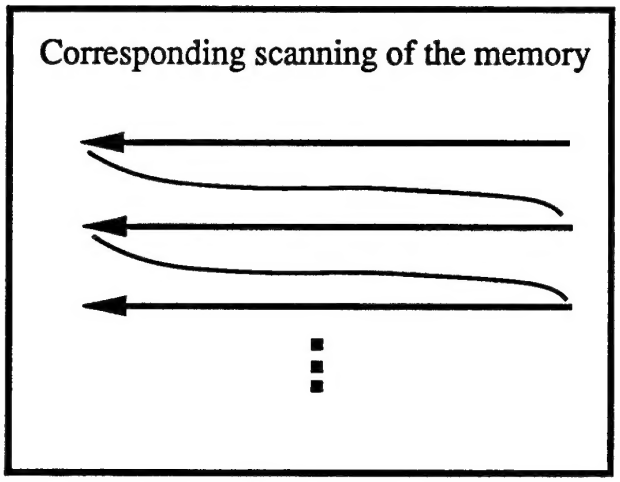


Pin #	Device	Function	Description
1			
2	n-ch transistor	Gate nMOS 3x3µm	
3	n-ch transistor	Drain nMOS 3x3µm	
4	n-ch transistor	Source nMOS 3x3µm	
5	64-bit SRAM	Vdd	Supply voltage (3 volts)
6	64-bit SRAM	INV3	Third bit (MSB) vertical decoder
7	64-bit SRAM	INV2	Second bit vertical decoder
8	64-bit SRAM	INV1	First bit (LSB) vertical decoder
9	64-bit SRAM	ENH	nable horizontal decoder (must be set to "0" to precharge all line
10	64-bit SRAM	OUT	Output
11			
12			
13			
14			
15			
16			
17	-	Back gate	-
18	p-ch transistor	Source pMOS 3x3µm	
19	p-ch transistor	Drain pMOS 3x3µm	
20	p-ch transistor	Gate pMOS 3x3µm	
21			
22			
23			
24			
25			
26			
27			
28			
29			
30			
31	64-bit SRAM	Vss	Ground
32	64-bit SRAM	ENV	Enable vertical decoder (must be set to "0" to precharge all lines)
33	64-bit SRAM	INH1	First bit (LSB) horizontal decoder
34	64-bit SRAM	INH2	Second bit horizontal decoder
35			
36			
37			
38	64-bit SRAM	INH3	Third bit (MSB) horizontal decoder
39	64-bit SRAM	IN	Input
40	64-bit SRAM	PRE	Dynamic precharge ("O"=precharge; "1"= no precharge)

Pin diagram for packages G53



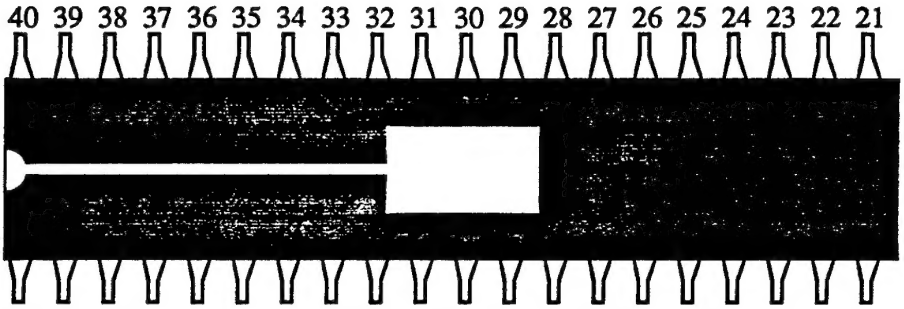
Above: precharge and read/write cycles for testing the SRAM. Below: corresponding scanning of the memory cells.



Above we propose a simple timing diagram for testing the SRAM. It consists of successively writing a "1", reading it, writing a "0", and reading it. This process is carried out for all cells. Therefore, the IN signal becomes alternatively high and low, and it is flipped during the READ operation (when ENV is low).

Both inputs ENH and ENV share the same diagram: when low, all the cells are disconnected from the lines and precharging occurs. When high, the dynamic precharge is disabled and the READ or WRITE operation is possible. The output is only valid during this short period. When using INV3 as MSB and IN1H as LSB, the memory is scanned from the right upper corner cell to the lower left cell.

Four of packages are labeled "M54" and "M55". They contain inverters of different types. The pin diagram of the packages is described below:



Pin #	Device	Function	Description
1			
2			
3			
4			
5			
6			
7			
8	Pull-up pair	Vdd	Vdd inverter with pull-up pair
9	Pull-up pair	OUT	Output inverter with pull-up pair
10	Diode pair	Vdd	Vdd inverter with diode pair
11	Diode pair	OUT	Output inverter with diode pair
12	Regular	OUT	Output regular inverter
13			
14			
15			
16			
17			
18			
19			
20			
21			
22			
23			
24			
25			
26			
27			
28			
29	Regular	Vdd	Vdd regular inverter
30	Regular	IN	Input regular inverter
31	All inverters	Ground	Common ground all inverters
32	Diode pair	IN	Input inverter with diode pair
33	Pull-up pair	IN	Input inverter with pull-up pair
34	-	Back gate	
35			
36			
37			
38			
39			
40			

Pin diagram for packages M54 and M55